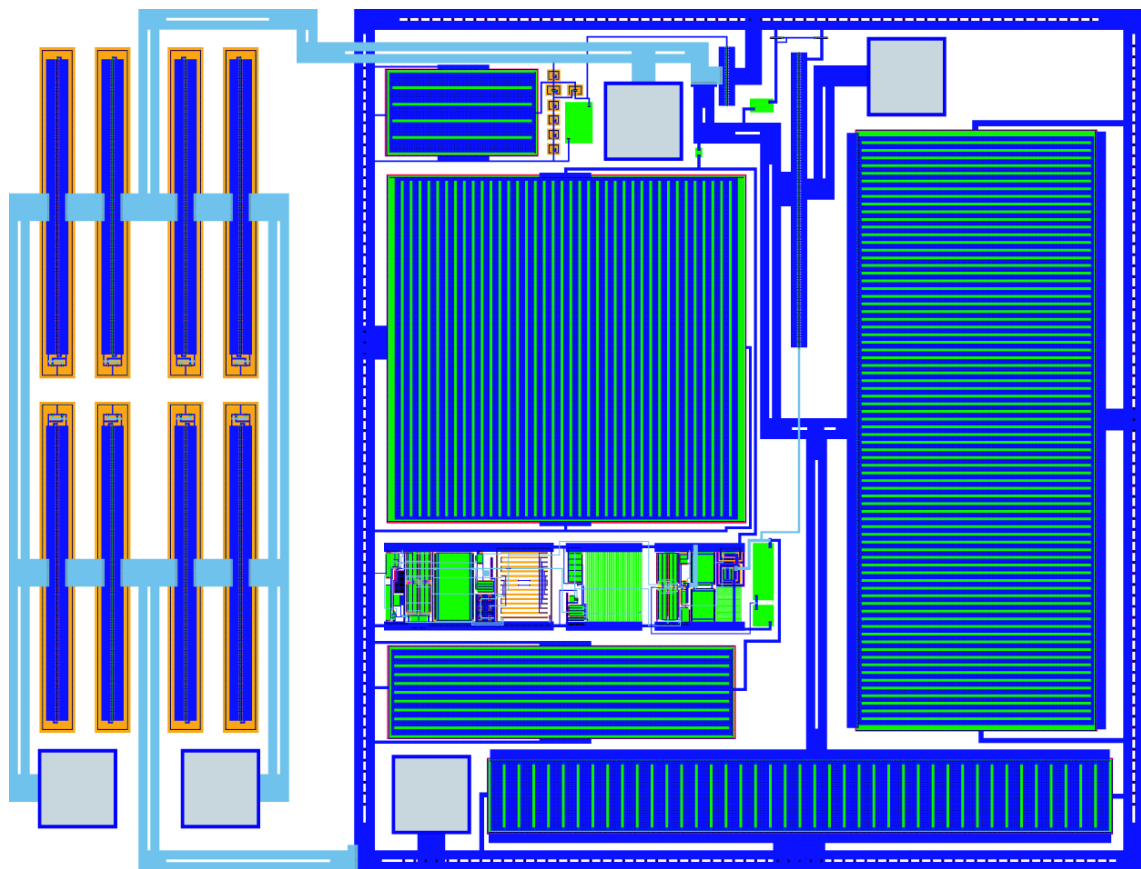


Diploma Thesis

# Wireless Power Supply and Data Transmission for Stress Sensor Systems



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# ABSTRACT

This diploma thesis describes the design of a CMOS interface which enables both, the wireless power supply of the *Smart-Bracket-System* and the wireless data transmission to an external base station. The *Smart-Bracket-System* is an integrated piezoresistive stress sensor system for orthodontic applications based on a commercially available  $0.6\ \mu\text{m}$  5V-CMOS process. It requires a supply voltage of 5 V and a maximum power of less than 30 mW. Restricted by the orthodontic application, its outer dimensions have to be smaller than  $2.5 \times 2.5\ \text{mm}^2$ . After several optimization and verification steps different wireless interface concepts were designed. Currently, they are fabricated in the same CMOS process as the sensor system.

The *Smart-Bracket-System* consists of two major components which are inductively coupled: (i) the external base station and (ii) the transponder chip including the wireless interface and the sensor system. The inductive coupling is based on an air-cored solenoid at the base station and a planar rectangular double layer coil placed at the top of the transponder chip. As highly efficient power transmission is required, the geometrical parameters of each coil were optimized with respect to the working frequency of the system (13.56 MHz). To enable such system optimizations, an analytical model of the inductively coupled *Smart-Bracket-System* was derived. In addition, this analytical model was used to simulate the consequences of resonance tuning inaccuracies for the system.

Three interface concepts for wireless power supply were realized: (i) a straightforward interface with an output voltage of 5 V, (ii) a 4.5 V interface optimized with respect to the signal quality of the output voltage and (iii) a low power interface with an output voltage of 3.3 V. Each interface consists of the same major components: (i) rectifier, (ii) voltage limiter and (iii) smoothing component. The rectifier was realized with PMOS transistors in diode configuration. To avoid parasitic leakage currents at the PMOS diodes, a dynamic bulk regulation was designed. The voltage limiter was realized with an electronic Zener diode consisting of several PMOS diodes connected in series. The optimized interface additionally contains a bandgap cell generating a reference voltage and a source follower working as buffer. The smoothing component was realized straightforwardly with poly-poly capacitors. Simulations on the entire system have shown that the optimized interface results in an output voltage ripple and a voltage shift both lower than 30 mV.

The layouts of the standard devices given by the CMOS foundry were redesigned with respect to a high current application. The designed final layouts of the interfaces are qualified for currents up to 30 mA and have a maximum area consumption of  $2 \times 1.5\ \text{mm}^2$ .

Taking the wireless data transmission to the base station into account, an ASK subcarrier load modulation concept was designed and simulated for the wireless interfaces. With respect to a testbench for the wireless interfaces, a straightforward concept for the base station was realized, tuned and characterized afterwards.

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