# Digital low-cost Time Domain Reflectometer circuit optimized for use in field applications

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**ABSTRACT**. Time Domain Reflectometry is a well-established method for measuring moisture profiles. In addition to special transmission lines this measurement principle requires a Time Domain Reflectometer. In the laboratory there are several state-of-the-art measurement devices available (e.g. Tektronix 1502B/C), but due to the high cost, the size and the power consumption they are often not suitable for field measurement applications. This article presents a new digital circuit design concept dedicated for developing cheap Time Domain Reflectometers especially suited for self-sustaining outdoor applications such as long-term field measurements.

**KURZFASSUNG.** Ein in der Feuchtemesstechnik bekanntes und etabliertes Messverfahren beruht auf der Zeitbereichsreflektometrie. Neben geeigneten Messleitungen erfordert dieses Messprinzip den Einsatz eines Zeitbereichsreflektometers. Im Labor stehen hierfür Messgeräte zur Verfügung (z.B. Tektronix 1502B/C), jedoch sind diese für Feldmessungen aufgrund der hohen Kosten, der Baugröße und des großen Leistungsbedarfs meist ungeeignet. Dieser Artikel zeigt ein neues digitales Schaltungskonzept zur Realisierung kostengünstiger Zeitbereichsreflektometer, insbesondere auch geeignet für den autarken Outdoor-Einsatz bei Langzeitmessungen.

*Keywords: TDR, Time-Domain-Reflectometry, Delta-Modulation*

## 1 Introduction

In many technical applications it is necessary to measure the moisture content of defined media such as soil [1, 2] or agricultural products [3]. In addition to the information about the moisture content the distribution of the moisture inside the media is often relevant. One well-known technique for measuring the spatial moisture distribution is Time Domain Reflectometry (TDR) [2, 4]. This measurement principle is based on electrical transmission lines which are embedded inside the media under investigation. A Time Domain Reflectometer (TDR-meter) is connected to the transmission line and generates electrical measurement signals such as repetitive rectangular pulses with sharp rising edges. The generated pulses travel along the transmission line until they reach the open end. During travelling along the line the generated waveform of the pulse is distorted due to dispersion and partial reflection because of the complex non-uniform transmission line impedance caused by the moisture. A reflection occurs at the end of the open line and the signal travels back to the generator. The TDR-meter captures the shape of the reflected signal which contains information about the moisture content along the transmission line [2]. Figure 1 shows an equivalent measurement setup replacing the TDR-meter by an arbitrary waveform generator (AWG) and a fast digital storage oscilloscope (DSO). The AWG generates repetitive pulses with sharp rising edges while the DSO continuously samples the voltage level at the entrance of the transmission line. The DSO must have a high sampling rate since the spatial resolution of the system depends on the temporal resolution of the DSO [2].

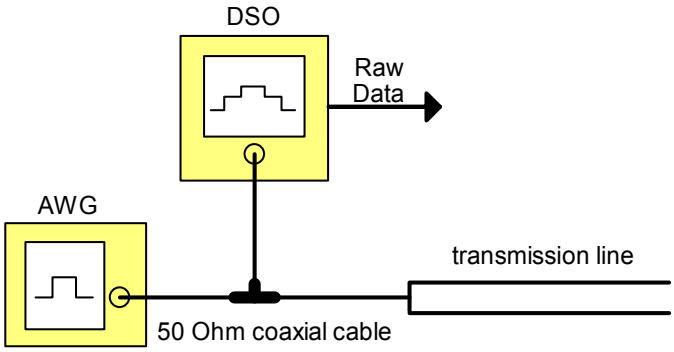


**Fig. 1:** Laboratory setup for TDR-measurements. The TDR-meter is replaced by an arbitrary wave-form generator (AWG) and a fast digital storage oscilloscope (DSO) which captures the shape of the reflected waveform. The characteristic wave impedance of the transmission line is matched to the coaxial cable and the generator's output impedance.

For experiments in the laboratory there are several state-of-the-art TDR-meters available like the Tektronix 1502B/C, the MOHR CT100 or the Campbell Scientific TDR100. Drawback of all available instruments is the high price, the size and the power consumption which often makes it difficult or even impossible to use these devices in outdoor field applications for autarkic long-term monitoring. A further drawback is the need for an external control device like a laptop computer for storing measurement data and for automating the measurement application. This article presents a new electrical measurement circuitry concept based on a revised Delta-Modulator (DM) structure as introduced in [2]. The new concept mainly uses pure digital components which greatly reduce the overall cost and increase the flexibility of the measurement circuitry. The use of an integrated microcontroller and a mass storage device like a SD-card as well as the very low overall power consumption make this concept ideally suited for building "lightweight" TDR-meters for cost sensitive high volume field applications.

## 2 Measurement Concept

The measurement circuit must be capable of replacing the AWG and the DSO shown in Fig. 1. While the generation of repetitive rectangular pulses is a straight forward task, the sampling process creates some difficulties. In order to achieve a high spatial resolution of the measurement system the sampling frequency must be high as well [2]. General drawback of a high sampling rate is the resulting high data rate which must be processed by the TDR-meter circuit and therefore significantly increases the system size, cost and power consumption. In order to optimize the electronic circuitry for low cost the proposed design employs a Delta-Modulator (DM) for capturing the measurement signal by a method often referred to as Equivalent Time Sampling (ETS). Since the moisture profile is a slowly changing physical variable in the system, it is feasible to capture the shape of the reflected signal by sampling many identical reflected signals instead of deriving all information out of one single pulse. Modifications of this method are often used in DSOs as well. In this article we propose a circuit which samples exactly 1 point of the waveform per excited measurement pulse. By continuously shifting the trigger signal relative to the repetitive measurement signal the circuit creates a "sweep" over the measurement signal. This sampling method reduces the required sampling rate to a frequency slightly below the measurement signal frequency and therefore greatly reduces the data rate which must be handled by the system. Tradeoff is the resulting extended measurement

time required to capture the full waveform. Since the moisture profile is quasistatic in comparison to the measurement time window of a few seconds the extended measurement time is acceptable in moisture measurement applications. Fig. 2 illustrates the described ETS-sampling process.

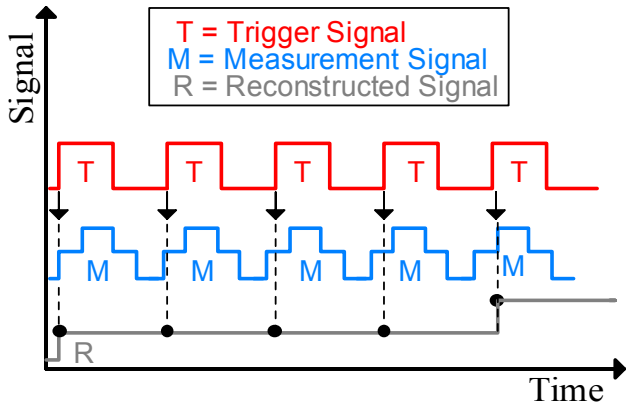


**Fig. 2:** Equivalent Time Sampling process illustrated for the resulting waveform of the reflected measurement signal (M). The trigger signal (T) frequency is slightly slower than the measurement signal frequency and therefore creates the "sweep" required to capture the signal. The resulting waveform (R) has the same shape as the sampled measurement signal (M) but on another time scale.

## 3 System Architecture

The measurement system block schematic is shown in Fig. 3. A low noise crystal oscillator generates a master clock frequency of 50 MHz. The generated master clock signal is divided into two path: the measurement signal path and the trigger signal path. In the measurement signal path the master clock frequency is divided by 32 using a fixed digital 5-bit counter implemented inside the Complex Programmable Logic Device (CPLD). The output frequency of the divider is therefore 1,5625 MHz. The frequency divider is followed by a line driver circuit which is capable of generating sharp rising edges and provides a matched output impedance for feeding the generated square wave pulses into the transmission line / TDR-probe. In the trigger signal path the master clock signal is used as input clock signal for a Direct Digital Synthesis (DDS) chip (Analog Devices AD9954). The DDS-synthesizer is used to generate the trigger signal frequency for the Delta-Modulator with a fine frequency resolution of 0,1 Hz. The sinusoidal output of the DDS-chip is filtered by a conventional analogue low pass filter and then shaped to a rectangular waveform for directly driving the CPLD trigger input pin of the Delta-Modulator. The Delta-Modulator itself consists of a binary counter inside the CPLD which is used as an integrator. On each incoming trigger pulse the integrator counts either up or down depending on the state of the external comparator output. The integrator's value is continuously fed back to the external comparator via a Digital-to-Analog converter. The comparator monitors the voltage level on the entrance of the transmission line and compares the state of the integrators actual value with the measurement signal level. As a matter of principal the output of the comparator is a serial pulse-code modulated bitstream which represents the shape of the measured signal. A shift register collects 8 databits and the resulting byte is either transferred to an external computer via a serial interface or stored in a memory device such as an SRAM or SD-card. The overall power consumption of the circuit is measured to be approximately 1,5 Watt in full operation mode. By simply switching off the power supply the overall power consumption can be reduced to zero. An

additional microcontroller (not shown in the block schematic) can therefore easily be employed to switch the system on or off on a defined cyclic basis for long-term field measurements. The remaining low supply current for the microcontroller is negligible when certain available low power modes are used. This allows for supplying the complete system out of a battery.

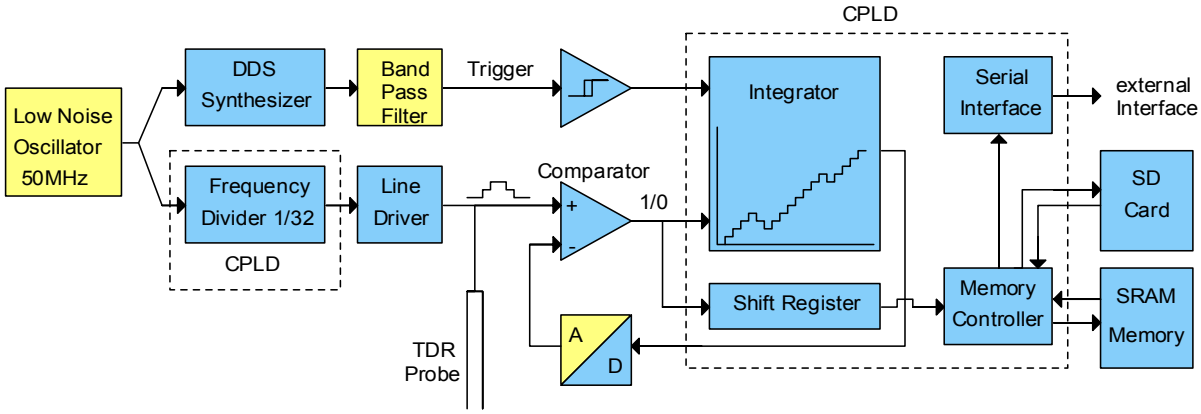


**Fig. 3:** Block schematic of the TDR-meter circuit. The system is mainly based on digital components (blue). Only very few components remain analogue such as filters and a high quality low noise oscillator for generation of the master clock frequency.

## 4 Delta – Modulator Principle

The following section gives a more detailed description of the employed Delta-Modulator functionality and the resulting behaviour in the system. As described above, the Delta-Modulator consists of a digital integrator, a comparator and an analogue feedback loop via a Digital-to-Analog converter. Input signals to the Delta-Modulator are the measurement signal (voltage level on the transmission line) and the trigger signal. Output of the Delta-Modulator is the serial bitstream of the comparator. Fig. 4 shows the structure on a more abstract level.

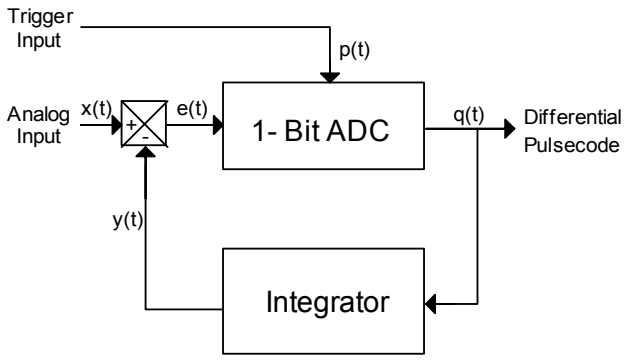


**Fig. 4:** Abstract signal flow inside the Delta-Modulator. The analogue input signal x(t) is compared to the integrator value y(t). The resulting difference is converted to digital domain by a 1-bit-Analog-to-Digital converter. The converter's output q(t) is integrated on each trigger pulse p(t) and fed back to the input. The output q(t) is a differential representation of the sampled input signal x(t).

In the implemented prototype version of the TDR-meter the repetitive measurement pulse signal has a frequency of approximately 1,5 MHz as described above. The trigger frequency $f_{trigger}$ generated by the DDS-synthesizer is adjusted to a frequency of 1,0 Hz below the pulse signal frequency $f_{pulse}$. According to equation (1) the resulting sweep time $t_s$ is 1,0 seconds for capturing the full waveform.

$$t_s = \frac{1}{f_{pulse} - f_{trigger}} \tag{1}$$

The resulting Delta-Modulator output is a serial bitstream with a data rate of 1,5 Mbit / s. Within the created measurement window of 1,0 seconds a total number of 1,5 million samples are taken. The total number of samples represent one full original waveform of the repetitive measurement signal. According to equation (2) the resulting theoretical equivalent temporal resolution $t_{res}$ is therefore 0,44 ps.

$$t_{res} = \frac{1 - \frac{f_{trigger}}{f_{pulse}}}{f_{pulse}} = \frac{1}{f_{pulse}} - \frac{f_{trigger}}{f_{pulse}^{\,2}} \tag{2}$$

## 5 Circuit Details

### 5.1 Measurement Pulse Generator Circuit

The pulse generation circuit mainly consists of one fast comparator ( TLV3501 ) with an output rise of approximately 2 ns and a following buffer. Because of the required fast slew rate of the measurement pulse a current feedback amplifier ( AD8009 ) is used. The circuit schematic is shown in Fig. 5. The input signal is filtered by a low noise high pass filter and directly fed to the comparator's inverting input. The positive input of the comparator is connected to a decoupled low noise reference voltage. In addition to a conventional constant hysteresis the feedback network creates a dynamic hysteresis to avoid multiple switching of the comparator. This is necessary because of the EMC-noise created by high dynamic peak currents which occur during the fast output transitions. The comparator output signal level is scaled down by a voltage divider network to prevent saturation effects in the output stage of the following operational amplifier. A series resistor on the amplifier's output is used to match the impedance of the transmission line.

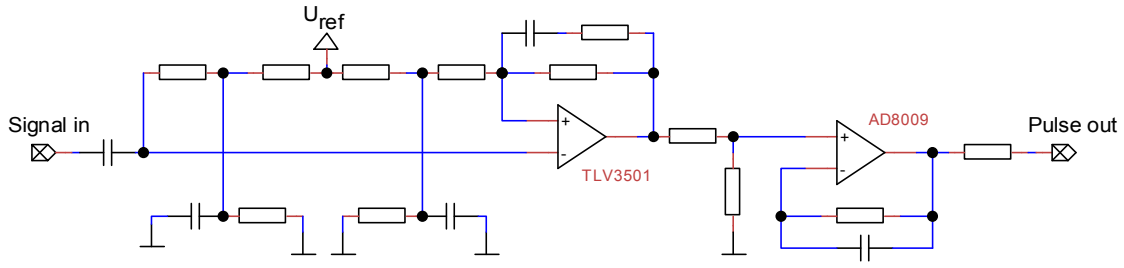


**Fig. 5:** Circuit schematic of the measurement signal pulse generator.

## 5.2 Sampling Comparator Circuit

The measurement signal is captured by a fast comparator ( TL3116 ). The comparator continuously compares the voltage level on the transmission line input (Analog Input) with the DA-converter output voltage in the feedback loop. Fig. 6 shows a more detailed schematic of the comparator circuit. The Delta-Modulator principle automatically creates a hysteresis via the discrete integrator steps and the resulting discrete analogue output voltage steps of the DA-converter. For this reason there is no further analogue hysteresis implemented in the circuit. For synchronization with the digital CPLD circuit the comparator's output is latched by the trigger signal. The chosen comparator has a latch-to-output time of 10 ns. A clock logic network implemented inside the CPLD generates appropriate timing signals for the internal integrator and the external DA-converter (Fig. 7). Since the CPLD is driven by the external 50 MHz master clock signal, the temporal resolution of the clock logic is 20 ns. The implemented circuit generates the "count-signal" (clk_i) for the integrator 40 ns after the rising edge of the latch signal of the comparator. This ensures a stable comparator output and an error free reading of the state. After reading the comparator's output the integrator immediately counts either up or down (1 = up, 0 = down). The actual integrator's value is continuously transferred to the external 14-bit DA-converter via 14 parallel lines. The clock logic generates a rising edge signal for the DA-converter input latch 40 ns after setting the data lines. In total the delay between the trigger signal and the DA-converter latch signal is therefore 2 x 40 ns = 80 ns. The trigger signal has a frequency of 1,5 MHz as described above. This is equal to a period of 666 ns. The remaining time of 666 ns – 80 ns = 586 ns allows for a stable settling of the DA-converter output and ensures a stable analogue feedback signal on the comparator's inverting input. The time constant of the low pass filter in the feedback network must match the timing requirements of the circuit.

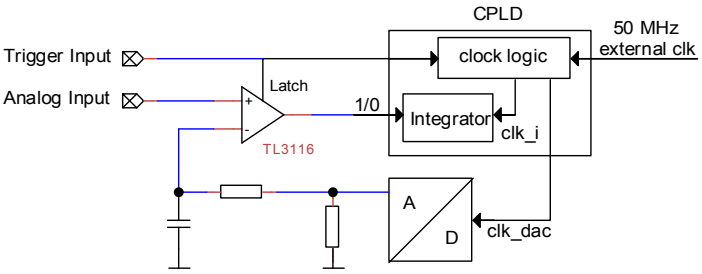


**Fig. 6:** Circuit schematic of the comparator which is used as 1-bit-AD-converter inside the Delta-Modulator. For synchronization with the digital logic implemented inside the CPLD a proper timing is crucial. The clock signal for timing the Delta-Modulator loop are generated inside the CPLD by a custom clock logic.

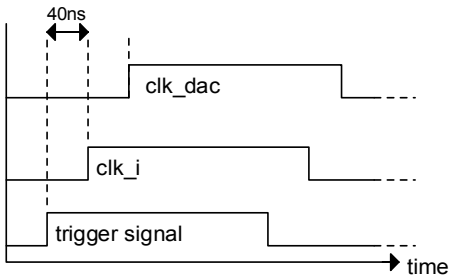


**Fig. 7:** Timing diagram of the clock signals generated inside the CPLD. The external trigger signal starts the timing process and latches the comparator. 40 ns after the latch signal the comparator output is read by the CPLD logic and the integrator is updated (signal "clk_i"). 40 ns later the DA-converter input latch is updated (signal "clk_dac").

## 6 Experimental Results

The developed prototype is tested in the laboratory and compared to conventional measurement equipment. The measurement setup is arranged as shown in Fig. 1. The AWG is a Tektronix AFG 3252 and the DSO is a LeCroy WaveRunner 104 Xi with a sample rate of 10 GS / s. The transmission line is replaced by a RG-58 type coaxial cable with a characteristic wave impedance of 50 Ohm and a length of 1,0 meters. The measurement is performed with an open unterminated cable. A comparison between the measured data shows a very good accuracy of the system (Fig. 8).

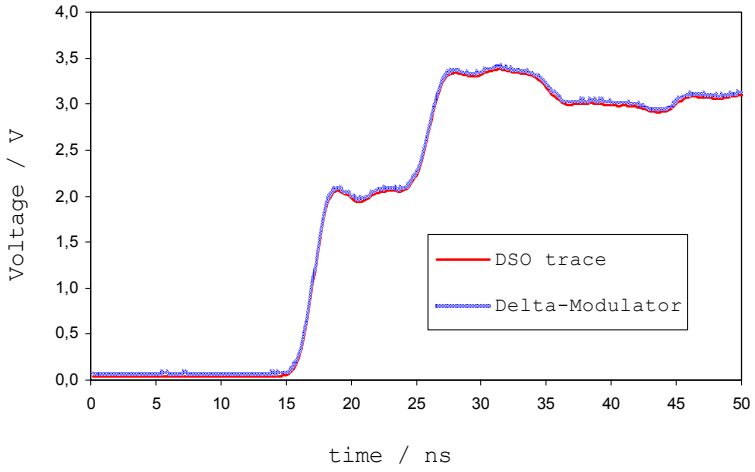


**Fig. 8:** Comparison of the laboratory measurement results derived from the developed Delta-Modulator circuitry and a conventional measurement setup using a digital oscilloscope. Both curves are almost identical which shows a very good resolution of the Delta-Modulator.

## 7 Conclusions and Perspective

The proposed TDR-meter circuit prototype shows a very good accuracy in the laboratory experiments in comparison to state-of-the-art equipment. The system concept is based on a Delta-Modulator structure which enables to transform the timebase of the excited measurement signal by undersampling and therefore leads to a very high theoretical temporal resolution of the sampling process. However, there are some practical limitations in the system. According to [2] a high slew rate of the rising and falling edges of the generated squarewave signal is important to obtain a good spatial resolution of the moisture distribution along the transmission line. In the prototype circuitry a conventional fast bipolar comparator is used to generate a sharp rising edge signal. The output of the comparator is buffered by a following high speed current feedback operational amplifier which certainly limits the achievable slew rate to approximately 2,0 V / ns. An other source of error in the system is the phase noise level of the trigger signal relative to the repetitive measurement signal. The theoretical temporal resolution of the developed prototype is better than 1 ps but due to jitter in the trigger signal the real resolution is in the range of 100 ps which equals a sampling rate of 10 GHz. The frequency divider in the measurement signal path already improves the phase noise level of the master clock oscillator by averaging the jitter of 32 clock periods but the trigger channel noise level depends on certain properties of the DDS-

synthesizer such as the DAC resolution and the oversampling rate as well as of the properties of the analogue filter following the output of the DDS-synthesizer.

In summary the proposed concept works very well. In further investigations the used CPLD will be replaced by a larger Field Programmable Gate Array (FPGA). This allows for replacing the conventional DDS-synthesizer chip by integrating an FPGA internal DDS-synthesizer application. Advantage of available DDS-cores for FPGAs is the achievable signal to noise ratio of the generated sinusoidal trigger signal of up to 115 dB due to mathematical optimizations like phase dithering and taylor series correction [5]. The generation of the sharp rising edges of the measurement signal will be optimized by employing fast CML-logic gates (e.g. Analog Devices ADCMP 572) which offer an output rise time of 35 ps for a 400 mV step signal [6].

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