Miniaturized FPGA-Based High-Resolution Time-Domain Reflectometer

Dennis Trebbels, Alois Kern, Felix Fellhauer, Christof Huebner, and Roland Zengerle

***Abstract*—Time-domain reflectometry (TDR) is a well-known measurement principle for evaluating frequency-dependent electric and dielectric properties of various materials and substances. Although TDR is a proven method, the high price for TDR measurement equipment and complex laboratory setups is often a limiting factor for cost-sensitive applications or large-scale field experiments, where a large number of TDR meters is required. This paper reports on the development of a new miniaturized low-cost TDR meter capable of sampling a repetitive rectangular waveform, which is used as an excitation signal. The developed sampling circuit is based on a digital delta modulator (DM) and allows for capturing the waveform of a repetitive measurement signal. A 1-MHz signal can be captured with a virtual sampling resolution of 1 ps within a measurement interval of 1 s. The generated pulses have a rise time of 2 ns and can be captured with an amplitude resolution of approximately 10 bit and an accuracy of approximately 8 bit. The developed digital DM architecture is implemented inside a small field programmable gate array and integrated into a miniaturized low-power TDR meter prototype for battery-powered outdoor applications. The captured measurement data are stored on integrated micro-SD card memory and can be read out either via a Universal Serial Bus, an RS-485 bus system, or a wireless interface. The TDR meter is controlled by an integrated microcontroller and a real-time clock and therefore can operate completely independent from any additional control setup. The TDR meter targets applications within the field of geoscience and agricultural monitoring, where large-scale measurement systems are required.**

***Index Terms*—Delta-modulation, time-domain reflectometry (TDR), undersampling.**

I. Introduction

TIME-DOMAIN reflectometry (TDR) is a well-known and common method for obtaining frequency-dependent electric and dielectric properties of materials and substances such as soil [1], [3], [4], [8], agro-food [2], grain [3], [4], snow [5], [8], wood [6], or concrete [7]. TDR is commonly based on transmission and reflection of a measurement signal, which contains high-frequency components with a bandwidth of several hundred megahertzs up to a few gigahertzs. Popular signals often found in existing TDR meters are rectangular square wave pulses with sharp rising edges or short needle pulses. The signal is fed into an application-specific waveguide probe such as open-ended coaxial lines or flat ribbon cables. Depending on the electric and dielectric properties of the material under test, partial reflections and dispersion occur along the probe or at the end of the probe. The resulting waveform of the signal is captured with a high temporal resolution, which is analyzed and interpreted depending on the specific application. In this paper, we focus on the development of a new TDR meter circuit, which is used in the field of geological and agricultural outdoor monitoring applications such as soil moisture measurement. In many cases, a long (up to 25 m) flat ribbon cable with a large fringing field is used as a waveguide and serves as a "sensor transmission line" [3], [5], [8]. Fig. 1 shows a ribbon cable, which is often used in geological TDR field experiments. The properties of the cable are analyzed in detail in [8]. Fig. 2 shows the expected characteristic wave impedance and the expected signal propagation velocity as a function of the permittivity of the surrounding medium. The permittivity correlates with the volumetric water content of the soil [8]. The open-ended cable is buried in soil, and the travel time of the injected signal is measured. The total travel time gives an integral value for the average moisture content of the soil along the line. As shown in Fig. 2, particularly at high water contents, the change in the relative signal propagation velocity becomes smaller. This requires capturing the signal travel time with a high temporal resolution and accuracy for detecting small changes in soil moisture.

Fig. 1. Flat ribbon cable with a characteristic impedance of approximately 200 Ω in air. The cable is buried, e.g., in soil, and the dielectric properties of the surrounding soil influence the characteristic impedance along the cable, which affects wave propagation and causes partial reflections.

In addition, there are some applications, such as groundwater monitoring, where a boundary layer exists between wet and dry soil. It is desired to locate the boundary layer with an accuracy of approximately ±10 cm and to monitor changes of the position of the boundary layer with a resolution of approximately

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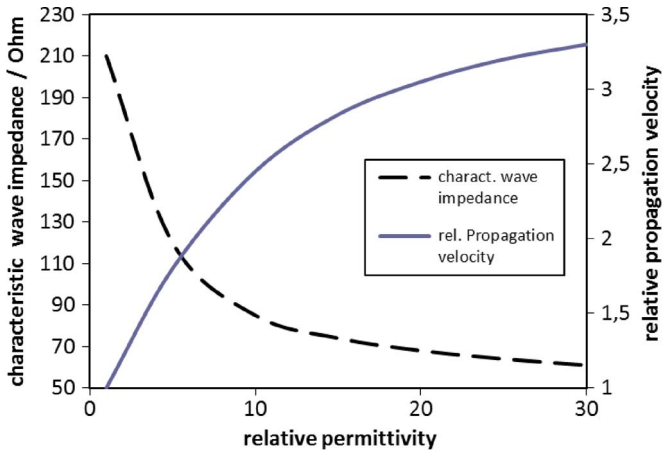

Fig. 2. Characteristics of the used flat ribbon cable shown in Fig. 1. (Solid line) Signal propagation velocity relative to the velocity on the cable "in air." (Dashed line) Corresponding characteristic wave impedance of the line. The impedance drops at a higher permittivity of the surrounding media.

1 cm. Estimating a typical travel time of 5 ns per meter, the resulting equivalent temporal resolution for 1 cm is 50 ps. Last but not least, there are some applications where a complete moisture profile along the transmission line is reconstructed out of the measured waveform [9]. Algorithms for reconstructing the moisture profile are far beyond the scope of this paper, but in general, it can be said that the amplitude resolution should be as good as possible. For precise reconstruction, the amplitude resolution and accuracy should be in the range of at least 8–10 bit.

Despite TDR-based measurement systems having been successfully used several times within research projects, there are almost no optimized TDR meters available on the market, which allows for a cheap and convenient widespread use of this technology, particularly in outdoor monitoring applications. The price of most well-known TDR meters such as the Tektronix 1502C, the Mohr Scientific CT100, or the Sympuls TDR 3000 typically is in the range of several thousand dollars. Furthermore, most available TDR meters are designed and optimized for laboratory use only and therefore have large housings, high power consumption, and are not well suited for outdoor use. Other TDR meters often found in geological and agricultural applications such as the Campbell Scientific TDR100 are intended for integration in automated measurement systems and require an additional external control setup such as a special data logger or a control computer. The overall measurement setup therefore becomes even more expensive and complicated. In large-scale field monitoring applications, it is often desirable to have a small TDR meter, which can be powered by a battery for a long time of several months and which does not require an external control setup. Such a TDR meter should be able to operate completely independent, performing cyclic measurements on a regularly timed basis and storing or transferring obtained data.

In the recent past, several concepts for new and innovative TDR meter circuits and systems have been presented. Lee *et al.* developed a random equivalent sampling TDR meter with a 16-ps sampling resolution based on needle pulse excitation [10]. According to their publication, the concept works well, but a drawback of the system is the requirement for two extremely stable crystal oscillators with very low frequency tolerances and a low-drift and well-known frequency in order to derive a defined sampling time base. Xudong *et al.* developed a TDR-based cable fault diagnosis system, but the system was implemented using expensive off-the-shelf laboratory equipment such as a pulse generator and a fast sampling oscilloscope [11]. Purisima *et al.* developed a field programmable gate array (FPGA)-based TDR system using prototyping boards, but due to the implemented direct sampling scheme, the temporal resolution is limited by the FPGA clock frequency to a few nanoseconds and therefore is very low compared with state-of-the-art TDR meters [12]. Negrea and Rangu introduced a small microcontroller-based sequential sampling TDR meter that employs three programmable delay lines for generating appropriate trigger signals for the sampling circuit. According to [13], the achieved temporal sampling resolution is only 250 ps. Schimmer *et al.* developed a portable high-frequency TDR meter that is capable of generating and capturing signals with very high frequency components up to a few gigahertzs [14], [15]. The system is also based on programmable delay lines. In this case, a strong drawback of the delay line concept is the limited number of programmable steps, which results either in a very limited overall recording time or in a limited temporal resolution, as already presented in [13]. In addition, delay lines have some more drawbacks such as high power consumption, the need for calibration, and, sometimes, limited availability on the market. Recently, Sokoll and Schimmer have improved their TDR sampling concept and replaced the programmable delay lines by two programmable but free-running oscillators [16]. The system shows an excellent performance and high accuracy up to very high frequencies in the gigahertz range. However, the developed system is optimized and intended for use with short waveguide probes such as open-ended coaxial lines. The system cannot easily be adapted for long transmission lines, as required in many geological and agricultural applications [17]–[19], due to the fact that the tuning accuracy of the free-running oscillators only allows for a rough frequency adjustment. As a consequence, the excited repetitive measurement signal must be kept in the range of several megahertzs in order to retain the excellent temporal resolution of a few picoseconds. Furthermore, the overall system is still expensive due to the optimization for very high frequency applications.

Despite all advancements and achievements made within the past years, there is still a lack of available low-cost TDR measurement equipment, which can easily be employed within large-scale outdoor field applications. Typical additional requirements for such an optimized TDR meter are very low power consumption, integrated measurement data storage, real-time clock based cyclic measurement intervals, and completely independent remote operation controlled by an internal microcontroller. For data readout, various interface types are desired such as a wireless transceiver, an RS-485 bus interface, and a Universal Serial Bus (USB). In this paper, we report on the design of a new digital TDR meter concept that fulfills these requirements while keeping total system cost at a very low level in the range of a few hundred dollars per TDR meter unit, which is approximately a factor of 10 cheaper than most currently available TDR meters.

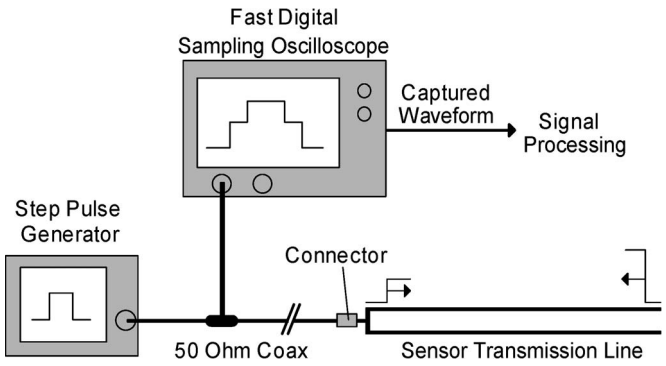

Fig. 3. Typical laboratory setup for TDR measurements based on a step pulse generator and a fast sampling oscilloscope for capturing the waveform.

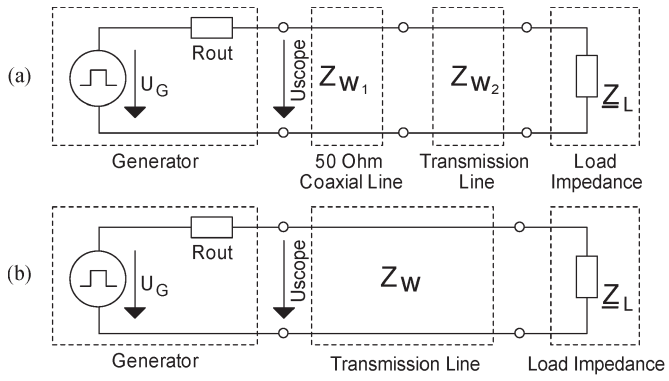

Fig. 4. (a) Equivalent electrical circuit model for the laboratory setup presented in Fig. 3. (b) Equivalent electrical circuit model for an optimized TDR system, where the generator is directly connected to the sensor transmission line and the generator output impedance matches the line impedance.

II. System Concept

The new developed TDR meter is based on repetitive rectangular pulses with a duty cycle of 50%. A voltage source with a defined output impedance (e.g., 50 Ω) excites the measurement signal, which is fed into an open-ended transmission line. The resulting voltage signal at the beginning of the line is sampled with a high temporal resolution. Fig. 3 illustrates the general concept based on a typical laboratory setup using a step pulse generator as a signal source and a fast digital sampling oscilloscope for capturing the waveform of the measurement signal. Fig. 4(a) shows the equivalent circuit model of the system. Fig. 5(a) illustrates the resulting typical waveform at the beginning of the line. The first rising edge at t_0 up to approximately $U_G/2$ in the signal is caused by the voltage divider formed by the generator output impedance R_{out} and the matching wave impedance Z_W of the coaxial line. After travelling along the coaxial line, the signal enters the connected flat ribbon cable. Due to impedance mismatching caused by the typically higher characteristic wave impedance of the flat ribbon cable, a partial reflection occurs. The partially reflected signal can be observed at t_1. The transmitted part of the signal travels along the ribbon cable and is distorted along the cable depending on the dielectric properties of the surrounding media (e.g., soil). After reaching the end of the open line, the signal is reflected and travels back to the generator. The last rising edge at t_2 can be observed at the beginning of the line. As illustrated in Fig. 5(a), only a small fraction of the signal contains relevant

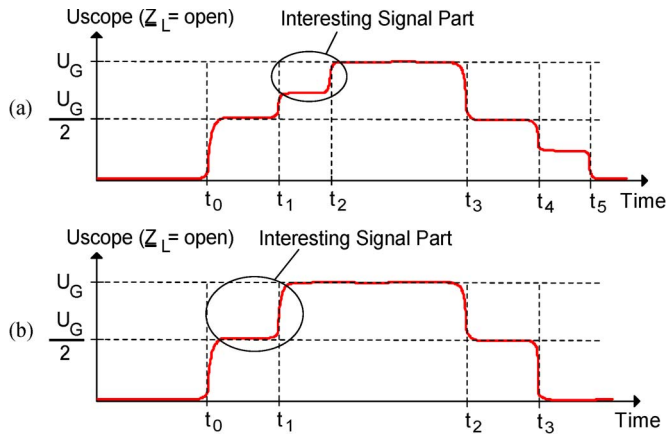

Fig. 5. Typical resulting waveforms that can be observed at the beginning of the transmission line. For simplification, multiple reflections are not drawn. The step pulse is generated and injected at t_0. (a) Typical signal expected from a sensor line, which is connected via a nonmatching coaxial feeding line. (b) Typical waveform for an ideal system with no feeding line and matched impedances between the sensor line and the generator.

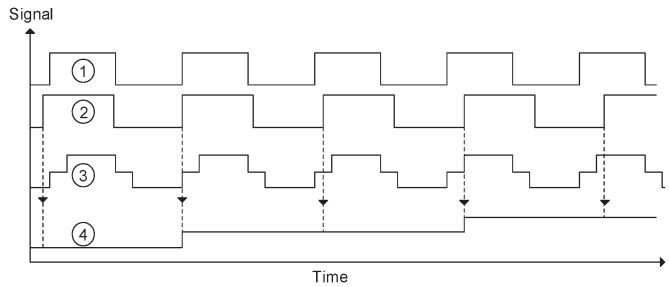

Fig. 6. Equivalent time sampling scheme, as implemented in the developed TDR meter. Two slightly different frequencies (signals 1 and 2) are required; one frequency is used as an excitation signal, and the second frequency is used as a trigger signal for the electronic sampling circuit. The sampled signal 3 is then reconstructed on a slower timescale (signal 4).

measurement information, and only a fraction of the vertical resolution is used. In an optimized TDR system, it is desired to directly connect the output of the generator to the input of the sensor transmission line. This allows for maximizing the injected signal energy by adjusting the output impedance of the TDR meter to the characteristic wave impedance of the sensor transmission line. A corresponding equivalent electrical circuit model is shown in Fig. 4(b), and the resulting typical waveform is shown in Fig. 5(b).

As a result of the impedance matching, the effective vertical resolution can be improved. However, to the knowledge of the authors, it is currently not possible to adjust the output impedance of available TDR meters. This point is taken into account for the new developed TDR meter.

III. Sampling Concept

A. Equivalent Time Sampling

The goal of the new TDR meter circuit is to capture a waveform with a high temporal resolution in the picosecond range. Direct real-time sampling is therefore not applicable. In order to reduce the sampling speed, we choose sequential equivalent time sampling as fundamental concept [20]. Fig. 6 illustrates the sampling process. Signal 1 is the generated step signal of the generator; signal 3 is the corresponding typical

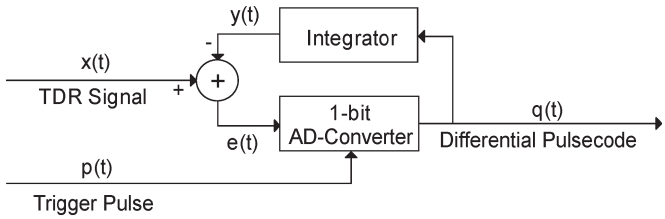

Fig. 7. Abstract block schematic of a DM. The input signal x(t) is digitized by the circuit and the output as digital pulse code modulated bit stream q(t). One sample (= one bit) is digitized on each trigger pulse p(t).

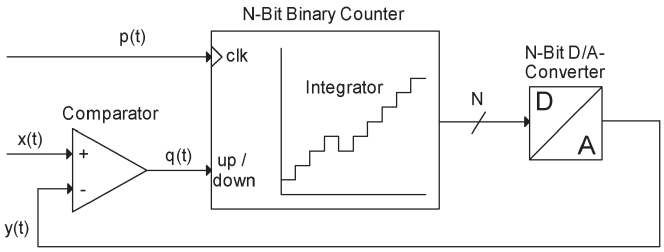

Fig. 8. Block schematic of the DM shown in Fig. 7, as implemented in the developed electronic sampling circuit. A comparator serves as a 1-bit A/D converter, and a binary counter serves as an integrator in the feedback loop.

double step signal at the beginning of the line. Signal 2 is a trigger signal with a slightly lower frequency than signal 1. On each rising edge of signal 2, one sample is taken of signal 3. Within each period of the repetitive signals, there is a short delay of the trigger signal, which results in sequentially "scanning" signal 3. The original signal 3 can be reconstructed out of the samples but on a slower timescale, as illustrated by signal 4. A more quantitative description of the method is given in Section III-C, where the system dynamics and the limitations of the developed TDR meter circuit are discussed.

B. Delta Modulation

As discussed above, on each rising edge of the trigger signal, one sample of the repetitive measurement signal is taken. In conventional sampling systems, there is usually a standard (analog-to-digital) A/D converter employed for digitizing the analog voltage level on the line. This conventional approach is straightforward and usually works fine, but a major drawback is the resulting huge amount of sampled raw data when capturing a signal with a very high temporal resolution. Storing and processing of large data sets is technically possible but, again, makes the overall system more complex and gives rise to the cost, size, and power consumption. In order to drastically reduce the amount of raw data, we replace a standard A/D converter by a digital delta modulator (DM). Such a DM-based concept has already been successfully introduced in [3] but was implemented as an analog circuit with some drawbacks and limitations, as well as resulting nonlinearities. An advantage of a DM is the fact that, instead of one n-bit absolute value per sample with an n-bit amplitude resolution, only the change of the signal amplitude between two following samples is encoded by 1 bit. This removes any redundancy and compresses the amount of sampled raw data by a factor n compared with a standard A/D converter with an n-bit amplitude resolution. For a 10-bit A/D converter, this means a 90% reduction in raw data. Fig. 7 shows an abstract model of a DM. Fig. 8 shows the corresponding block schematic of the DM as implemented in the developed electronic circuit. The measurement signal x(t) is continuously compared with a feedback signal y(t) by a fast comparator, which serves as a 1-bit A/D converter. On each incoming trigger signal p(t), the output q(t) of the comparator is latched, and depending on the state of the output, an integrator (digital counter) in the feedback loop is forced to either count up or down. The closed-loop structure forces the integrator to virtually continuously track the measurement signal x(t) but on a much slower timescale. A quantitative description is given in Section III-C. The bit stream output of the comparator q(t) is the pulse code modulated form of the signal x(t), which is equivalent to the derivative of x(t).

C. System Dynamics and Limitations

The resulting virtual temporal resolution of the equivalent time sampling circuit and the resulting system dynamics of the DM depend on the fundamental measurement signal repetition frequency f_{pulse} and the fundamental trigger signal frequency f_{trigger}. By controlling both frequencies, the temporal resolution of the system can be adjusted. The total acquisition time t_s required to capture one full period of the measurement signal by sampling one sample per period is

$$t_s = \frac{1}{f_{\mathrm{pulse}} - f_{\mathrm{trigger}}} = \frac{1}{\Delta f}. \tag{1}$$

The achieved virtual temporal sampling resolution t_{res} can be calculated by

$$t_{\mathrm{res}} = T_{\mathrm{trigger}} - T_{\mathrm{pulse}} = \frac{f_{\mathrm{pulse}} - f_{\mathrm{trigger}}}{f_{\mathrm{pulse}} \times f_{\mathrm{trigger}}}. \tag{2}$$

The combination of (1) and (2) leads to the following expressions for the acquisition time t_s and the required delta frequency Δf as a function of the measurement signal frequency with the given parameter t_{res}:

$$t_s = \frac{1}{f_{\mathrm{pulse}}} + \frac{1}{f_{\mathrm{pulse}}^2 \times t_{\mathrm{res}}} \tag{3}$$

$$\Delta f = \frac{f_{\mathrm{pulse}}^2 \times t_{\mathrm{res}}}{f_{\mathrm{pulse}} \times t_{\mathrm{res}} + 1}. \tag{4}$$

In an equivalent time sampling system with extensive undersampling, Δf is usually much smaller than f_{pulse}, which allows us to simplify (3) and (4) to (5) and (6) by assuming that $f_{\mathrm{pulse}} = f_{\mathrm{trigger}}$. Equations (5) and (6) show that there is quadratic dependence between t_s or t_{res} on one side and f_{pulse} on the other side, i.e.,

$$t_s = \frac{1}{t_{\mathrm{res}} \times f_{\mathrm{pulse}}^2} \tag{5}$$

$$\Delta f = t_{\mathrm{res}} \times f_{\mathrm{pulse}}^2. \tag{6}$$

However, the following sections are based on (3) and (4).

Fig. 9 is a plot of (3) for three selected sampling resolutions t_{res} of 1, 10, and 100 ps equivalent to virtual sampling rates of 1000, 100, and 10 GHz, respectively. The graph in Fig. 10 is a plot of (4) and shows the required delta frequency Δf between the measurement signal and the trigger signal for the same three selected sampling resolutions t_{res}.

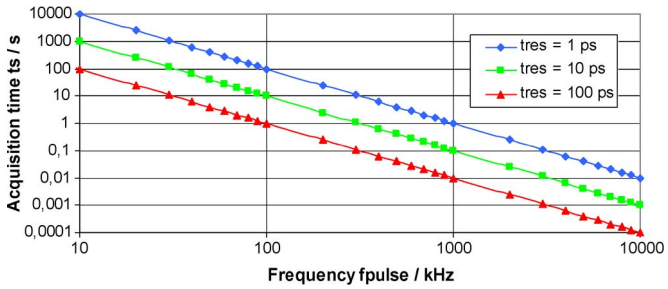

Fig. 9. Resulting acquisition time t_s for capturing one period of the measurement signal as a function of the measurement signal frequency f_{pulse} for three selected temporal sampling resolutions t_{res}.

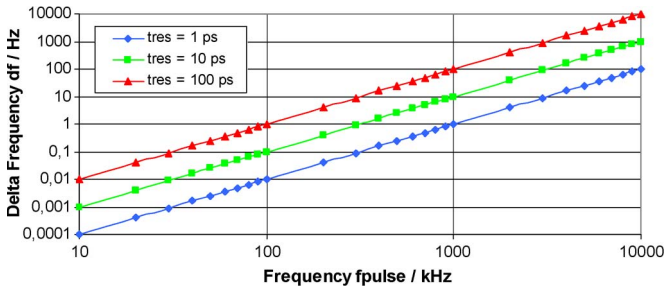

Fig. 10. Required delta frequency Δf as a function of the measurement signal frequency f_{pulse} for three selected temporal sampling resolutions t_{res}.

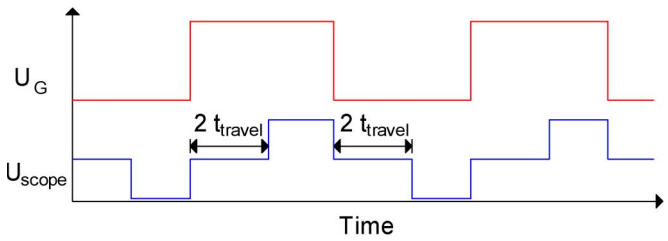

Fig. 11. In an ideal system without multiple reflections and without ringing on the transmission line, the maximum measurement signal frequency is given by the length of the line and the resulting travel time of the signal on the line.

Figs. 9 and 10 clearly show that the equivalent time sampling concept works very well for higher frequencies in the megahertz range, whereas lower frequencies result in a long acquisition time when a high virtual resolution is required. Therefore, on the first view, it looks attractive to choose a high measurement signal frequency. However, there are commonly two more practical limitations for the measurement signal frequency. The first limitation is the travel time of the signal on the transmission line. It is desired to excite a new pulse into the line only when the previous pulse is over and the line is "free" in order to avoid superposing of multiple pulses. For a transmission line with, e.g., a 10-m length, as often used in soil moisture measurement applications, the travel time in one direction will be approximately 50 ns depending on the exact line characteristics. For a 50-ns travel time, the theoretical limit of the measurement signal frequency is $1/(4\ t_{\mathrm{travel}}) = 5$ MHz. The resulting waveform for an ideal system according to Fig. 4(b) with an open-ended line is shown in Fig. 11. The period of the measurement signal must be greater than four times the travel time of the signal into one direction of the line.

The second practical limit for the measurement signal frequency is given by the timing of one closed-loop cycle according to Fig. 12. One complete loop cycle is illustrated in Fig. 12. The first time constant in the loop, after exciting the trigger signal (which is a latch signal for the sampling comparator), is a mandatory fixed delay, which must be waited for in order to ensure a stable and settled comparator output. Since the integrator is continuously virtually tracking the input voltage level, the differential input signal of the comparator at the latch signal moment is always very low and in the millivolt range. Therefore, the comparator latch setup time always becomes relatively large. In the developed prototype design, we allow for a 100-ns latch setup time, which is a factor of at least 10, compared with the typical latch setup times of a few nanoseconds of fast bipolar comparators. After the setup time, the output of the comparator is read by the FPGA, where the digital counter is implemented. For internal synchronization and processing, five FPGA clock ticks are required, which is equal to 100 ns in our design. Then, the (digital-to-analog) D/A converter is updated with the new integrator value. The D/A converter and following amplifiers require a certain settling time until the analog output value is stable. In total, the "loop time" is 500 ns in our circuit, which limits the maximum trigger signal frequency to $1/500$ ns $= 2$ MHz. As a compromise between acquisition time, temporal resolution, and transmission line length, we choose 1 MHz as the fundamental repetition frequency of the TDR signal. A detailed investigation of the expected measurement accuracy and resolution is presented in the experimental section.

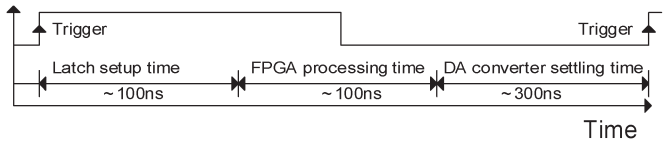

Fig. 12. Timing diagram for one complete loop cycle. Major delays within the loop are the sampling comparator latch setup time, the FPGA processing time, and the D/A converter output settling time.

Due to the time constant of the integrator in the feedback loop, there is another theoretical limitation. On one hand, it is desired that the amplitude resolution of the captured waveform is good (e.g., in the range of 8...12 bit). On the other hand, it is desired that the DM can follow signals with a high slew rate such as the sharp rising edges of the injected square wave signal. In case of a DM, the behavior of the integrator in the feedback loop does not allow for optimizing the circuit in such a way that both requirements are fulfilled at the same time. In practical applications, it is necessary to make a compromise between the maximum slew rate and the amplitude resolution of the feedback signal. The only applicable solution to increase the amplitude resolution while keeping a defined maximum slew rate is to increase the sampling resolution t_{res} of the system. This is theoretically possible by adjusting the delta frequency Δf but will lead to a longer acquisition time, as already discussed earlier (see Fig. 9).

The minimum rise time t_{rise} of a full-scale step signal, which can still be followed by an n-bit integrator, which can perform $n-1$ steps, is

$$t_{\mathrm{rise}} = (2^n - 1) \times t_{\mathrm{res}}. \tag{7}$$

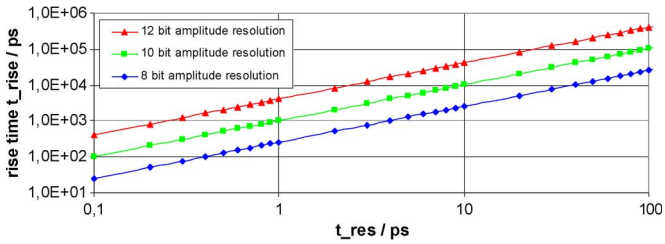

Fig. 13. Minimum full-scale step signal rise time, which can be tracked by the DM loop as a function of the temporal sampling resolution t_{res} for different amplitude resolutions.

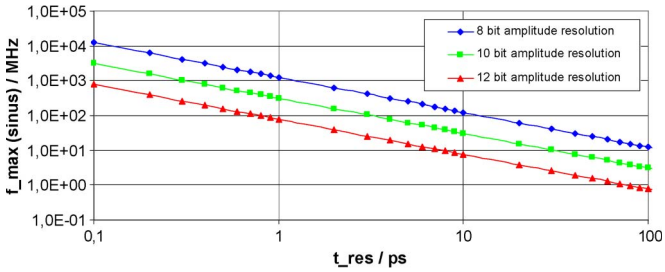

Fig. 14. Maximum frequency f_{max} as a function of the temporal sampling resolution t_{res}, which can be sampled in case of a sinusoidal measurement signal with an amplitude covering the full dynamic range of the integrator in the feedback loop.

The graph in Fig. 13 illustrates this behavior for several amplitude resolutions as a function of the temporal sampling resolution. For a sinusoidal signal with an amplitude equal to the dynamic range of the DM circuit, this means a maximum frequency f_{max}, which can be captured by the system, i.e.,

$$f_{\mathrm{max}} = \frac{1}{\pi(2^n - 1) \times t_{\mathrm{res}}}. \tag{8}$$

Higher frequency sinusoidal signals can only be captured by reducing their amplitude, but this results in less amplitude resolution because, then, the fixed dynamic range of the feedback loop is not fully used. The graph in Fig. 14 shows the maximum theoretical frequency for sinusoidal signals with a full amplitude, which can be captured as a function of the temporal resolution for different amplitude resolutions.

As aforementioned, we chose a square wave signal with 1 MHz as fundamental frequency and a temporal resolution of 1 ps as a compromise between the resulting amplitude resolution and the required acquisition time. Fig. 15 shows the resulting theoretical minimum full-scale step rise time as a function of the achievable amplitude resolution according to (7). However, in our circuit, the rise time of the signal is limited by the slew rate of the line driver circuit for amplitude resolutions below 11 bit. For amplitude resolutions above 11 bit, the rise time is limited by the integrator.

IV. Electronic Circuit

The developed prototype circuit is divided into three subcircuits. The main circuit contains a small-size FPGA, a microcontroller for system control and operation, SRAM memory, a real-time clock (RTC), and some interface components for connecting the digital processing hardware to the analog front end. The analog front end consists of a line driver circuit, which

Fig. 15. Minimum rise time as a function of the achievable amplitude resolution for a virtual temporal sampling resolution of 1 ps. In the developed circuit, the rise time is limited to 2 ns by the line driver slew rate for amplitude resolutions below 11 bit. For amplitude resolutions above 11 bit, the rise time is limited by the integrator time constant.

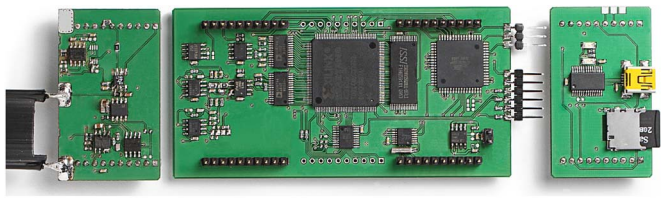

Fig. 16. Photograph of the developed miniaturized TDR meter circuit. The size of the main board in the middle is 100 × 50 mm. The two circuit boards on the side (left: line driver and sampling circuit, right: communication interfaces) are designed as header boards and can be mounted on top of the mainboard.

is able to excite pulses into a transmission line, as well as the comparator-based DM sampling circuit. For data storage and connection to a computer, a separate circuit board with various communication interfaces such as USB, RS-485, and 868-MHz wireless transceivers is developed. An on-board micro-SD card allows for storing up to 2 GB of measurement data. Fig. 16 shows a photograph of the developed circuit boards. Fig. 17 shows a comprehensive block schematic of the TDR meter. Fig. 18 shows a fully assembled prototype with cable. Almost all important system functions are implemented within the FPGA, except for the external large SRAM memory for temporary data storage and a "housekeeping" microcontroller. The microcontroller controls the FPGA via a custom Serial Peripheral Interface. The microcontroller is connected to a programmable RTC, which allows for using the TDR meter as an independent remote measurement device that can perform measurements on a cyclic basis. The microcontroller is waked up by an RTC interrupt and organizes a full measurement cycle. After completing a measurement cycle and storing the obtained data, the microcontroller shuts down the power supply for most components on the printed circuit board (PCB) and falls back to a power-saving sleep mode. While sleeping, the total current consumption at a supply voltage of 6 V is below 10 μA, which allows for a long time supply via a small battery pack. During active measurement with a 50-Ω transmission line connected to the output, the current consumption is approximately 190 mA, but only for a period of approximately 1 s until the TDR meter circuit is switched off by the microcontroller again. In order to save power, it is desired to keep the acquisition time as short as possible.

According to (4) and Fig. 10, the delta frequency Δf between the measurement signal and the trigger signal must be very small when a high temporal resolution is required. For a

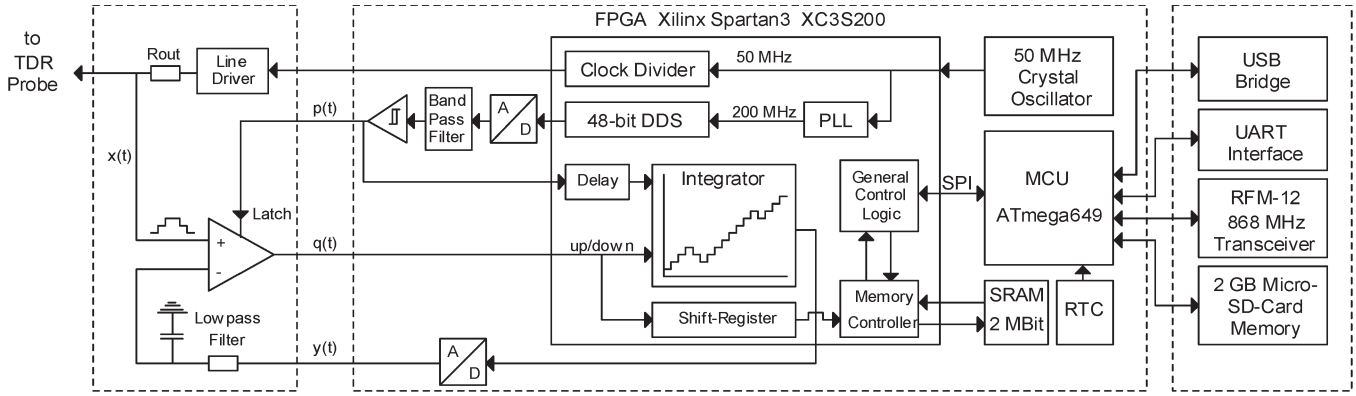

Fig. 17. Block schematic of the complete electronic TDR meter circuit. Almost all measurement functionalities are implemented inside a small standard FPGA. A microcontroller controls all functionalities, including the FPGA, the SRAM memory readout, the data storage, and the data transmission via various interface types. The small analog part consists of a line driver circuit and the sampling comparator-based DM circuit.

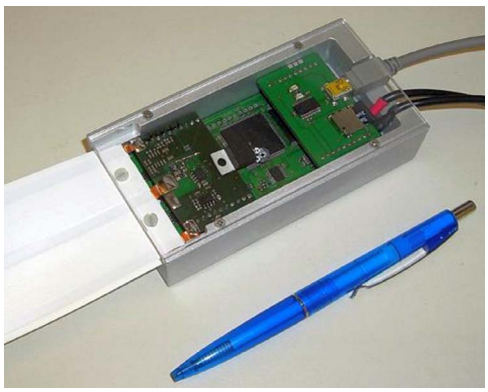

Fig. 18. Photograph of the fully assembled TDR meter. The electronic circuit is encapsulated in a custom-made housing. A flat ribbon sensor cable is directly connected to the TDR meter by soldering the cable ends on the PCB.

1-MHz measurement signal, Δf must be 1 Hz when a virtual resolution of 1 ps is desired, which is equal to 1-ppm relative frequency tuning accuracy. The fundamental measurement signal frequency f_{pulse} is derived from the 50-MHz FPGA system clock by a decimal divider counter. The trigger signal is also derived from the same 50-MHz clock time base but can be precisely adjusted by a direct digital synthesizer (DDS), which is also implemented inside the FPGA. The frequency tuning accuracy is defined by the 48-bit wide internal phase accumulator of the DDS and the DDS clock frequency, which is 4×50 MHz $= 200$ MHz. The resulting tuning accuracy is $200\ \mathrm{MHz}/2^{48} = 0.71\ \mu$Hz. The output of the DDS related D/A converter (AD9744) is filtered by a good LC bandpass filter with a quality factor $Q = 80$ in order to further reduce harmonics and therefore reduce the sampling jitter. The filtered DDS output signal is converted to a square wave signal by a Schmitt trigger circuit using a fast comparator (LT1711).

The pulse code modulated serial bit stream q(t), which represents the sampled signal, is processed by a memory controller unit and is transferred to external SRAM for temporary storage. Up to 2 Mbit can be stored inside the SRAM, which is equal to a recording time of 2 μs with a resolution of 1 ps. This long recording time is sufficient for transmission lines having a length of up to approximately 200 m, which is already much longer than used in most practical applications.

The line driver circuit is shown in Fig. 19. The square wave measurement signal is shaped by a fast bipolar comparator (LT1711). The comparator reaches a rise time of 2 ns for a pulse with an amplitude of 5 V. The generated 5-V pulse is reduced to a 3-V pulse by a voltage divider and then buffered by a following fast current feedback amplifier. Reduction of the pulse amplitude is necessary to keep the signal amplitude within a certain input voltage range of the sampling comparator. The transmission line is connected to the output of the buffer amplifier via an additional output resistor R_{out}. This resistor can easily be replaced by any resistor (greater than 50 Ω) for achieving optimized impedance matching between the TDR meter output impedance and the characteristic line impedance. The achieved rise time of 2 ns is slower than many state-of-the-art TDR meters can reach, according to their datasheets. In some applications, this may not be acceptable, e.g., if a short coaxial probe is used as a transmission line. However, in the field of geological and agricultural soil monitoring applications, the used transmission lines are usually long and in the range of several meters. In addition, the specified short rise time of state-of-the-art TDR meters is often a more theoretical value, which can be directly measured at the output of the TDR meter. If the TDR meter is connected to a flat ribbon cable via a 50-Ω coaxial feeding line (e.g., RG 58), the rise time of the injected pulse is significantly degraded within the first few meters of the coaxial line. In addition, there are, often, RF multiplexers used to connect multiple sensor lines to one TDR meter. Inserting such an additional RF multiplexer causes additional slew rate degradation. However, in most practical target applications for the new TDR meter, a 2-ns rise time is fully acceptable. On the other hand, the use of a standard comparator as a pulse source offers the great advantage of having a large step signal amplitude of 3 V, which is approximately a factor of 10 higher than in most other TDR meters. In theory, the pulse amplitude is not so important, but in the case of the above presented sampling circuit, this is an advantage because the input hysteresis of the sampling comparator is very small compared with the signal amplitude. In the laboratory, we figured out that most fast bipolar comparators have an internal input hysteresis in the range of 1–3 mV, which is often not fully specified in the datasheet. In the case of a low signal amplitude, this effect may degrade the sampling amplitude resolution. In the case of a

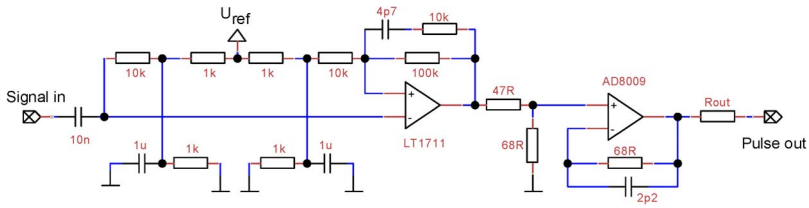

Fig. 19. Schematic of the line driver circuit. A fast bipolar comparator is used to form a square wave with sharp rising edges from the input signal. The achieved slew rate is approximately 2 ns for a 5-V step signal. The comparator output is buffered by a fast current feedback amplifier, which drives the connected transmission line via the matched output resistor R_{out}.

3-V step signal, we can almost ignore this minor effect as it becomes only relevant if high amplitude resolutions better than approximately 10 bit are required for the raw data acquisition.

The sampling circuit comparator requires only few components and is illustrated in Fig. 17 on the left side as a part of the analog header board. The comparator must have a high analog input bandwidth, a wide input voltage range, a latch input with a short latch setup time (a few nanoseconds are preferred), and a short propagation delay to ensure fast sampling and readout. In the prototype circuit, we successfully used the LT1711 comparator. The analog feedback signal y(t) is low-pass filtered with a filter located close to the input pin of the comparator in order to reduce coupled electromagnetic compatibility noise caused by the fast switching components on the PCB. The cutoff frequency of the low-pass filter is 5 MHz to ensure that there is no significant additional phase shift between the analog DM output signal and the comparators input at the time of the rising edge of each latch signal. In addition, to a careful PCB layout, every analog comparator and amplifier is supplied by an individual stabilized power regulator in order to prevent ripple on the individual power rails and thus reduce induced noise in the circuit to a minimum. The result is a very clean excitation signal without noticeable distortion caused by short switching peak currents. This short time stability of the signals is mandatory for correctly capturing a repetitive signal without distortion. Long time stability issues such as temperature drift do not play a significant role during one measurement cycle because the acquisition time is only a fraction of a second.

V. Experiments

The developed TDR meter circuit is tested in the laboratory and during a groundwater monitoring field experiment. The laboratory experiments are done to investigate the general system accuracy, repeatability, and resolution. The field experiment is done in order to test the developed system under real conditions.

A. Laboratory Experiment 1: Accuracy and Resolution

The first experiment is a comparison to a conventional laboratory setup as shown in Fig. 3. The goal of the experiment is to test the amplitude accuracy of the system at different fundamental excitation signal frequencies. In particular, the behavior of the sampling comparators input stage is of major interest since the input signal level covers the entire input voltage range. Typical effects such as (virtual) offset voltages and gain errors caused by the limited common-mode rejection ratio of the sampling comparator have to be evaluated.

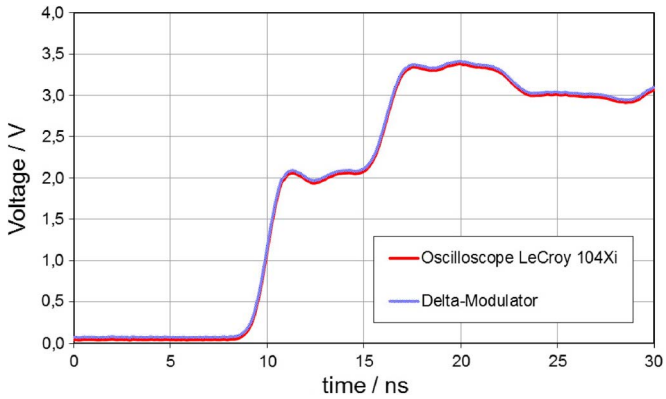

Fig. 20. Comparison of the captured waveforms of a TDR measurement using an open-ended coaxial cable. One curve is sampled with an oscilloscope (LeCroy Waverunner 104 Xi), and the second curve is captured with the new developed TDR meter.

The output resistor R_{out} is set to 50 Ω, which allows for comparing the device to other standard laboratory equipment having 50-Ω outputs. In addition, it allows for connecting a 50-Ω coaxial cable for defined and reproducible measurements. For this experiment, the amplitude resolution is set to 10 bit, and the virtual sampling resolution is set to 1 ps. According to Fig. 13, a full-scale step pulse with a minimum rise time of 1 ns can be captured with these settings. The generated pulse has a measured rise time of approximately 2 ns; thus, there is still some margin to ensure that the integrator can virtually track the input signal despite the presence of some jitter. The experiment is done four times. In each experiment, the fundamental excitation signal frequency and, thus, the required trigger frequency are changed. We are investigating the system behavior at 100 and 500 kHz and 1 and 2 MHz. Frequencies lower than 100 kHz lead to extremely long acquisition times and are not acceptable in our target applications. Even at 100 kHz, the acquisition time is already 100 s when a temporal resolution of 1 ps is desired. Frequencies higher than 2 MHz cannot be handled by our electronic circuit mainly because of the required loop time for each sample, as explained in Section III (see Fig. 12). In the experiment, the transmission line is an open-ended RG-58-type coaxial cable with 50-Ω characteristic wave impedance. For reference, the TDR signal is captured with a fast digital oscilloscope (LeCroy Waverunner 104Xi). The vertical resolution of the oscilloscope is 10 bit. Ten curves are recorded and averaged. Both traces are compared with each other, and the difference is computed to see if there are deviations from each other. As an example, Fig. 20 shows two resulting averaged waveforms in one plot. The data were

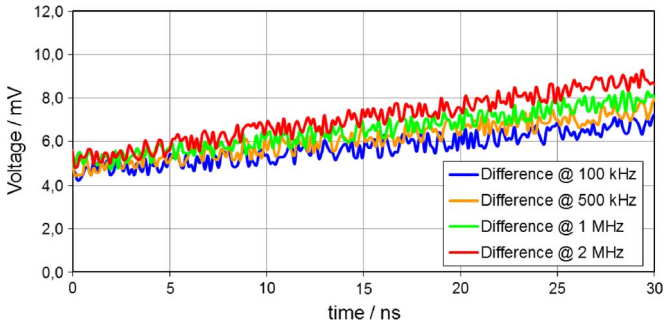

Fig. 21. Difference between sampled curves. For each frequency, one curve is sampled with a digital oscilloscope, and the other curve is sampled with the TDR meter circuit. The graph shows a gain error of approximately 5–9 mV and additionally superposed noise with an amplitude in the range of 1 mV.

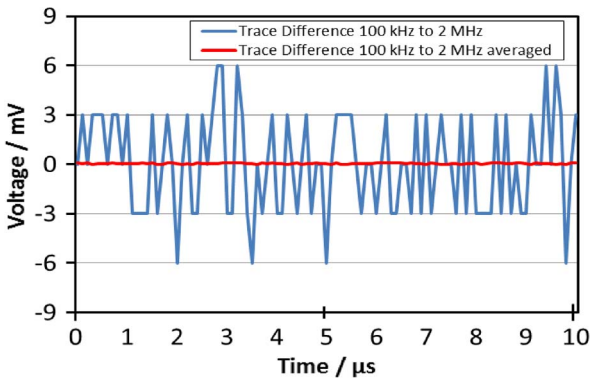

Fig. 22. Difference between two sampled curves of the excitation signal. One curve is sampled at a fundamental excitation signal frequency of 100 kHz; the second curve is sampled at 2 MHz. Both curves are sampled with the digital oscilloscope. Applying a moving averaging filter with a width of 128, samples to the raw data show that the difference is almost perfectly zero, which means that the excitation source is stable at the tested frequencies.

obtained at 1 MHz. Both curves are almost identical and are matching very well. Fig. 21 shows the difference between the curves sampled with the TDR meter and with the oscilloscope for all four tested frequencies. It is obvious that there is a gain error of a few millivolts. The gain error is not constant but increases at higher input signal levels. In particular, at higher fundamental frequencies, the increase in the measured gain error is higher. At 2 MHz, the measured error is already in the range of 9 mV. A test of the sampling comparator shows that its dc input offset voltage is approximately 4 mV. In order to exclude a frequency-dependent excitation signal degradation or distortion of the signal source, we compare the excitation signal full scale output level sampled with the oscilloscope at 100 kHz and 2 MHz. The difference is shown in Fig. 22. The visible noise is in the range of ± 3 mV, which is equal to 1 bit at a 3-V excitation signal amplitude and a full-scale vertical resolution of 10 bit of the oscilloscope. Since there is no remarkable difference, the signal source is stable over the tested frequency range, and the observed gain error is most likely caused by a slightly decreased performance of the comparators input stage at higher frequencies and at higher common-mode levels of the input signal. However, in total, this experiment shows that the vertical accuracy of the developed TDR meter is in the range of 8 bit without any offset or gain error compensation and approximately 9 bit when we mathematically reduce the measured gain error by subtracting a constant offset (the dc offset voltage) of the comparator. The ripple found on all four sampled curves in Fig. 21 is approximately 1 mV. As aforementioned, the curves are averaged curves from ten measurement cycles. In theory, the ripple is at least one least significant bit of the feedback loop resolution, which is approximately 4.0 mV in this experiment for a 4.0-V full-scale digital-to-analog converter amplitude and 10-bit amplitude quantization. It can be concluded that the sampling resolution of the system is in the same range as the integrator resolution in the feedback loop.

TABLE I
THE TABLE SHOWS THE MEASURED AMPLITUDE ERROR OF THE CAPTURED MEASUREMENT SIGNAL FOR DIFFERENT COMBINATIONS OF OUTPUT IMPEDANCE AND TRANSMISSION LINE WAVE IMPEDANCE

R_out / Ohm	R_load / Ohm	Error % @ 100 kHz	Error % @ 500 kHz	Error % @ 1 MHz	Error % @ 2 MHz
49.2	0	-0,40	-0,03	-0,33	-0,10
	50.5	0,06	-0,16	-0,38	0,13
	102.1	0,27	-0,37	-0,16	0,16
	204.4	0,48	0,39	0,27	0,39
	1019.1	0,38	0,20	0,18	0,40
101.6	0	-0,30	-0,41	0,27	-0,48
	50.5	0,34	0,00	0,48	-0,17
	102.1	0,21	-0,39	0,17	-0,44
	204.4	-0,43	0,46	0,23	0,15
	1019.1	-0,32	-0,21	-0,43	0,19
199.0	0	-0,16	-0,49	0,33	0,14
	50.5	-0,09	-0,27	0,05	-0,22
	102.1	-0,40	-0,06	-0,31	0,33
	204.4	-0,42	-0,42	0,44	-0,34
	1019.1	-0,11	0,47	0,08	-0,21

B. *Laboratory Experiment 2: Accuracy and Load*

In a second laboratory experiment, the amplitude accuracy is further verified under different load conditions. In this experiment, a resistor is directly soldered to the output pads of the TDR meter circuit instead of a transmission line and forms a voltage divider with the output resistor R_{out} of the TDR meter circuit. The sampled voltage level is compared with the theoretical voltage level, which we expect for the known voltage divider. The amplitude error between the theoretical and measured signals is computed. As explained in Section IV, the output resistor of the TDR meter can be varied in order to adapt to different transmission lines with different characteristic line impedances. In this experiment, we set R_{out} to nominal values of 50, 100, and 200 Ω, which is in the range of typical TDR transmission lines. As a load resistor, in each case, we connect nominal values of 0, 50, 100, and 200 Ω and 1 kΩ. Since all resistors have initial tolerances, the resistors are measured, and the test results shown in Table I are computed with the exact values. The presented result is always the error in percent with respect to the theoretical value. All measured combinations show an amplitude error below $\pm 0.5\%$, many samples below $\pm 0.25\%$, which is equal to an amplitude accuracy in the range of 8 bit for all tested load and frequency combinations.

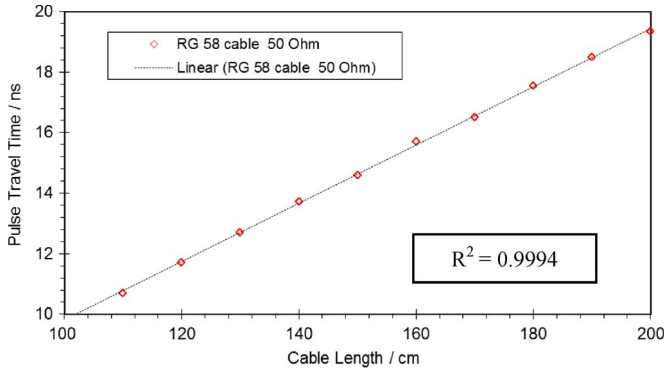

Fig. 23. Measured pulse travel time as a function of the cable length. The cable is shortened by 10 cm for each measurement. The expected graph is a linear function. With $R^2 = 0.9994$, the TDR meter circuit shows an excellent linearity.

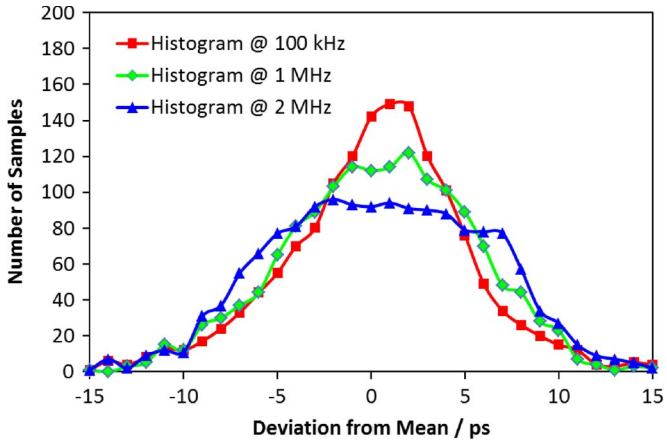

Fig. 24. Envelope functions of the jitter histograms for the two fundamental excitation frequencies of 100 kHz and 2 MHz. The resulting jitter is slightly lower at 100 kHz, but the difference in the two envelope functions is of minor importance with respect to the required accuracy of the TDR meter within the target applications.

C. Laboratory Experiment 3: Time Base Linearity

In a third laboratory experiment, the linearity of the time base of the new circuit is tested. At the beginning of the experiment, an open-ended 50-Ω coaxial cable with a length of 200 cm is connected to the TDR meter. The travel time of the signal is measured and averaged ten times by capturing the TDR waveform and comparing the captured signal level to the two threshold values of 1/4 U_G and 3/4 U_G in order to locate the two rising edges of the characteristic double step signal. Then, the coaxial cable is shortened by 10 cm, and the measurement is repeated. The experiment was done ten times until the cable was shortened to 100 cm. Shortening the cable can be done with high accuracy and ensures that other components such as the connectors remain constant during the experiment. The measurement result is presented in Fig. 23. With $R^2 = 0.9994$, the circuit shows an excellent linearity. One reason for the achieved excellent linearity is the continuously running sampling concept based on a DDS clock generation. In contrast to delay lines, there is no inherent nonlinearity present. The only source of timing errors created by the DDS clock system is spurs in the DDS output spectrum, which occur due to a limited DDS sampling frequency, a limited amplitude resolution of the D/A converter, and jitter of the DDS driving clock signal. The implemented DDS synthesizer has a measured spurious-free dynamic range of approximately 70–75 dB when generating output frequencies in the range of 100 kHz–2 MHz. All spurs are further reduced by a sharp LC bandpass filter. The remaining spurs will directly be translated to sampling jitter by the following comparator, which forms a square wave out of the sinusoidal DDS output. The square wave signal is required for triggering the latch input of the sampling comparator. The jitter effects are analyzed and discussed below.

D. Laboratory Experiment 4: Jitter Estimation

Jitter will affect the effective sampling resolution and accuracy and, potentially, will limit the minimum rise time of a step signal, which the integrator must be able to follow. In this system, the relevant sampling jitter means timing imperfections of the latch signal relative to the measurement pulses. In the system, there are several sources that potentially cause timing jitter. As aforementioned, the most important sources are spurs in the DDS output signal and switching jitter caused by the comparator, which converts the sinusoidal DDS output to a square wave signal. In addition, there is the switching jitter of the line driver circuit, the jitter caused by a nonconstant latch setup time of the sampling comparator, and, of course, the initial jitter from the crystal oscillator and the following FPGA clock distribution and clock management modules such as the internal phase-locked loop and the clock divider. All timing jitter effects add up in the system and may randomly cancel out each other or result in a worst case jitter scenario where all jitter effects add up into one direction. Since it is difficult to directly measure each source of jitter without influencing the circuit, we performed a further experiment to investigate the total amount of jitter. Within the test, the output resistance R_{out} was set to 50 Ω, and an open-ended coaxial cable of type RG-58 with a length of 2 m and a characteristic wave impedance of 50 Ω was connected. The lowest output resistance is 50 Ω, which can be driven by the line driver. The fast switching output currents are high in this case, and therefore, the switching noise is expected to be high as well. We use this configuration as a worst case scenario. The experiment is done three times with the fundamental excitation frequencies of 100 kHz and 1 and 2 MHz in order to investigate the frequency dependence of the jitter effects. During each experiment, the TDR meter circuit performed 1500 complete measurements of the resulting characteristic curves [see Fig. 5(b)]. The equivalent time between the internal start signal for the excited pulse and the first matching of the sampled signal amplitude with a compare value of 3/4 U_G was recorded. Out of the 1500 performed measurements, a jitter histogram for each sampling frequency was derived. Fig. 24 shows the envelope curves of the three histograms. It can be seen that the resulting jitter effects are lower at 100 kHz than at 1 or 2 MHz. One reason is that the DDS generator has a higher oversampling rate in this case, which leads to a better spurious-free dynamic range. Another reason is that transients in the circuit

such as fast switching currents at 100 kHz have 20 times more time to decay than at 2 MHz. However, the difference between the derived envelope functions is of minor importance for the overall performance of the TDR meter with respect to the requirements set by our target application. The shape of the histograms is not a perfect Gaussian function. However, the total amount of jitter is significantly smaller than the required sampling resolution of the target application of approximately 50 ps. For this reason, it is not necessary to further investigate the individual jitter sources.

The measured jitter is bigger than the actual virtual sampling resolution of 1 ps. However, it is still useful to keep the 1-ps resolution in the system in order to allow the integrator to track rising edges with a rise time as low as approximately 1–2 ns while keeping the amplitude resolution at a level of 10 bit. The amplitude resolution in the system is better than the accuracy. In several applications, this is absolutely useful when only the ratio between two amplitudes is important and the absolute value is of minor interest. As discussed in Section III-C, the integrator in an ideal system can track signals with a rise time of 1 ns with an amplitude resolution of 10 bit when a virtual temporal sampling resolution of 1 ps is adjusted. The implemented line driver is limited to a rise time of 2 ns, but it is still useful to keep a 1-ps virtual resolution in order to suppress rise time limitations caused by jitter and to have some margin to the theoretical boundary. From Fig. 24, it is obvious that the sampled output of the system cannot be used for applications where a real 1-ps resolution is required. However, the sampling specification for the target application is in the range of 50 ps, as discussed in Section I. In addition to the resulting high amplitude resolution of the system, the oversampled waveform allows for optional additional low-pass filtering by applying a moving averaging filter with a limited width. If the width of the filter is smaller than the number of samples, which occurs during the step rise time, there is almost no remarkable effect on the slew rate degradation.

E. Field Experiment: Groundwater Monitoring

The developed TDR meter circuit is used within a field experiment for groundwater monitoring. The transmission line shown in Fig. 1 is vertically installed into a bore hole in sand ground with a length of 4 m. The TDR meter is encapsulated into a water-resistant housing, and the transmission line is directly connected to the PCB. In the field experiment, the output resistor R_{out} is set to 150 Ω to achieve a better match with the characteristic wave impedance of the used transmission line. The transmission line impedance is expected to be in the range of approximately 100–200 Ω depending on the soil moisture (see also Fig. 2). The goal of the experiment is to measure the groundwater level by evaluation of the sampled TDR signal. It is expected that the characteristic line impedance changes at the boundary layer between dry sand and wet sand, which will result in a partial reflection of the injected signal and create a typical step in the sampled curve. The expected shape of the curve is similar to that in Fig. 5(a) with three rising edges. The first rising edge is caused by the voltage divider created by R_{out} and the transmission line impedance in dry sand. The second

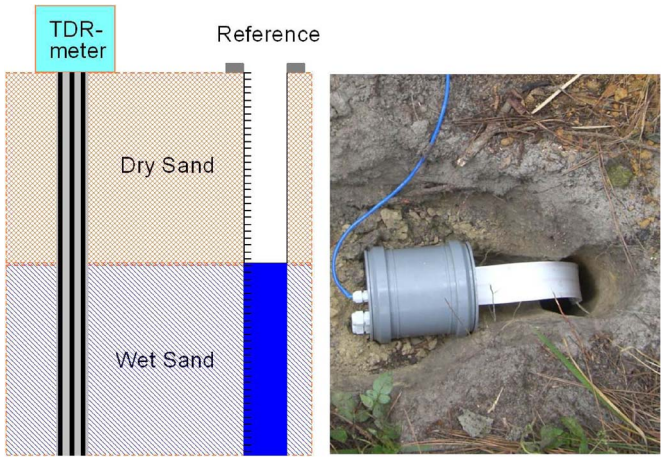

Fig. 25. Field experiment measurement setup. The picture on the left shows the installation of the transmission line in the sand ground. The picture on the right shows a photograph of the TDR meter circuit encapsulated in a water-resistant housing and directly attached to the transmission line, which is inserted into a bore hole. After insertion, the bore hole is filled with sand again.

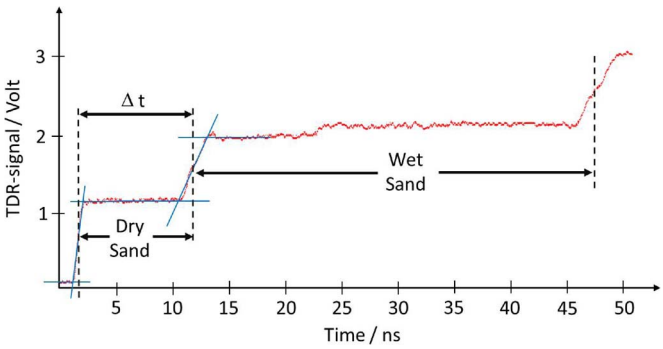

Fig. 26. Data evaluation of the sampled TDR profile of the field experiment shown in Fig. 25. The characteristic steps in the signal are located, and tangents are fitted to the signal. The curve before and after the steps is fitted by two horizontal lines. The mid of the tangent between the two intersection points is taken as a measure for the position of the step.

rising edge is created by the superposition of the partially reflected wave at the boundary layer between dry and wet sand, which causes a change in the transmission line impedance. The third rising edge occurs because of the superposition of the reflection caused at the open end of the transmission line. The experimental setup is illustrated in Fig. 25. The sampled TDR curves are analyzed in order to locate the position of the typical rising edges. The difference Δt between the first and second rising edges gives information about the position of the boundary layer between dry and wet sand in the ground. Fig. 26 shows one typical sampled curve and illustrates the applied analyzing methods. Tangents are fitted to the rising edges in the signal. The curve right before and after the rising edges is approximated by two horizontally fitted lines. The mid of the tangent between the resulting two intersection points is taken as a measure for the position of the rising edges. In order to calculate the equivalent distance to Δt between the first two edges, it is required to know the propagation speed of the signal on the line. The propagation speed on our used transmission line can be derived from Fig. 2 if the corresponding characteristic wave impedance in dry sand is known. The characteristic wave

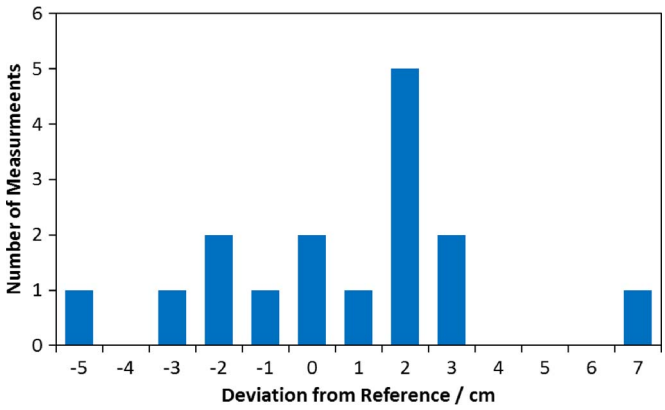

Fig. 27. Histogram for 16 groundwater level measurements. The histogram shows the absolute deviation to the reference measurements. The mean value of the deviation is +0.69, and the standard deviation is 2.77. The accuracy of the reference is approximately 1.0 cm.

impedance can easily be calculated by the height of the first rising edge because it depends on the voltage divider effect between the line and the well-known value of the output resistor R_{out} of the TDR meter circuit. We performed several measurements with the experimental setup. The TDR meter was configured to a 1-MHz fundamental excitation signal frequency and a 1-ps virtual temporal resolution with the integrator resolution set to 10 bit. As a reference, we used a conventional bore hole, where we could measure the water level manually with an accuracy of approximately 1.0 cm. Fig. 27 shows a histogram for 16 measurements and its absolute deviation in centimeters compared with the reference method. All measurements are within our targeted accuracy of ± 10 cm; the mean value of the deviation is $+0.69$, and the standard deviation is 2.77.

VI. Conclusion

The new developed miniaturized TDR meter circuit is based on several well-known methods such as equivalent time sampling, delta modulation, and precise DDS frequency generation. The overall circuit concept combines many attractive advantages of these single techniques in a smart way. The result is a very flexible and scalable measurement unit, which can easily be adapted to application-specific needs in terms of virtual sampling rate, fundamental step signal frequency, amplitude resolution, and acquisition time. The fundamental measurement signal frequency of the repetitive excitation signal can be adjusted independently of the temporal resolution; only the acquisition time will vary. The equivalent time sampling scheme is a tradeoff between the acquisition time and a very high virtual temporal sampling rate. Advantages of the sequential sampling method are the low overall complexity and the low real-time data rate, which must be processed by the circuit. A new digital sampling circuit based on a DM architecture further reduces the overall system complexity and the resulting amount of sampled raw data by pulse code modulation. Due to the mainly digital character of the system and the reduced complexity, it is possible to integrate the bigger part of the design into a small FPGA.

In the implemented prototype circuit, we tested frequencies in the range of 100 kHz–2 MHz. Frequencies below 100 kHz result in a very long acquisition time. Frequencies above 2 MHz cannot be processed by the developed circuit due to timing limitations. The laboratory experiments show that the jitter effects become more visible at higher fundamental excitation signal frequencies. However, we decided to choose a 1-MHz fundamental measurement signal frequency and a 1-ps virtual temporal resolution for our field experiment as a compromise. The accuracy and resolution at 1 MHz fulfill our target application requirements. An advantage of the 1-MHz excitation signal frequency is that the acquisition time is by a factor of 100 lower than at 100 kHz while keeping the same temporal resolution. In our target application, where the TDR meter is supplied by a battery, this saves a great amount of energy.

The new TDR meter eliminates all major conceptual drawbacks of delay-line-based sampling systems such as a limited recording time or a fixed sampling resolution by using continuous signals with fine relative frequency adjustment options given by the DDS. The rise time of the generated step output signal is approximately 2 ns when driving a 3-V step signal into a 50-Ω cable. The rise time is currently limited by the line driver stage, which is based on a fast comparator and a fast operational amplifier. For the targeted measurement applications in many geological and agricultural experiments, the achieved slew rate is sufficient. In addition to the limited slew rate, the only further tradeoff, as compared with established laboratory TDR meters, is the slower acquisition speed, but in many cases, this is not relevant.

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