Semiconductor devices and technology

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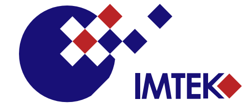
Lecture overview



- 1: Introduction & hist. overview
- **2: Silicon crystal growth**
- 3: Oxidation of Silicon
- 4: Lithography
- 5: Advanced Lithography
- 6: Wet Etching
- 7: Dry Etching
- 8: Doping & Diffusion
- 9: Ion Implantation
- 10: Epitaxy & CVD
- 11: PECVD & ALD
- 12: Metal-Gate Processes
- 13: Wafer Cleaning
- 14: CMOS Processing
- 15: Packaging/Outlook
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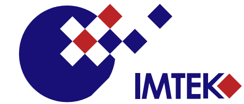
- 17: Crystal structure
- 18: Energy Bands and Conductivity
- 19: pn – junctions
- 20: MOSFET
- 21: LEDs
- 22: Solar Cells
- 23: Lasers
- 24: Photodetectors

Silicon technology - overview



An integrated circuit has now 10^6 transistors and related connections and interconnections which are produced on the surface of single crystalline wafers based on a number of process steps.

Si wafers have now the size of up to 12 inch (~30 cm, the size of a "pizza")

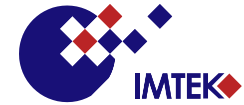
Complex systems are reliably build, with high cost efficiency (process cost per wafer the same, but functionality increases, smaller line width…)

At the same time 100 copies or more of the circuits are built up.

Why silicon become the most significant semiconducting material?

- Low cost material (27% of the earth is Silicon)
- High quality surface oxide
- Easy to produce oxide films

Silicon technology - overview



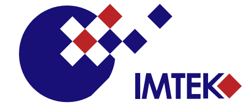
Silicon → Silicon Wafers

Layout → Photo Masks

Packages

Silicon Wafers + Photo Masks → Silicon Technology Wafer Processing

Silicon Technology Wafer Processing + Packages → **Integrated Circuit**

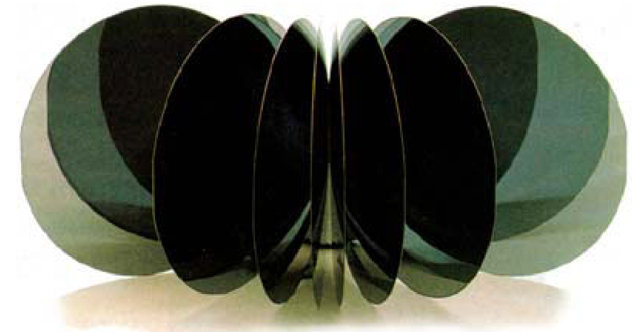


Silicon technology - overview

Production of poly (polycrystalline) silicon

Wafer production

Growth of single crystals

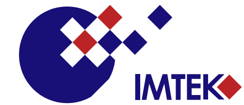


Wafer slicing

Surface finishing: Lapping and polishing

Semiconductor structuring

Silicon technology - overview



Oxidation

Spinning of photo resist

Repeated lithography/ retro chips

Epitaxy

Stepper exposure

Developing

Etching

Wafer production

Lithography

Semiconductor structuring & wafer processing

Rinsing, drying

Film deposition

Packaging

Resist strip

Metal etching

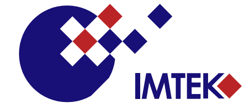
Metallization

Copper deposition

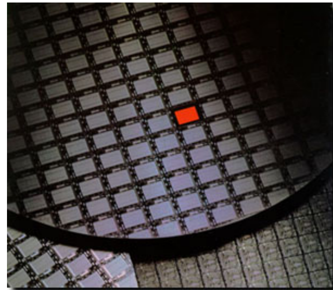
CVD

Ion implantation

Silicon technology - overview



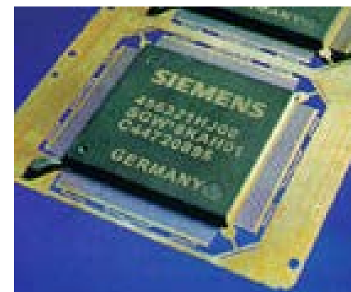
Semiconductor microstructuring



Wafer prober & Die slicing (single bare chips)

Chip packaging processes

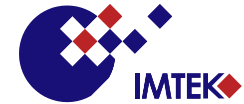
Electronic connections & contacts:
Die bonding & wire bonding

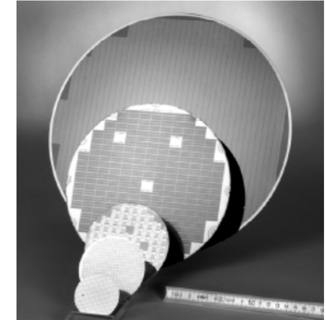


Mounting, packaging

Die (dies, dices)- bare Die - bare chip

Si crystal growth



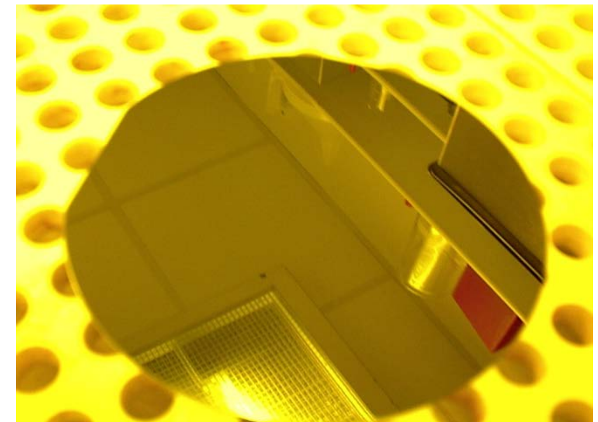


Parameter (ultra pure single crystalline silicon wafers):

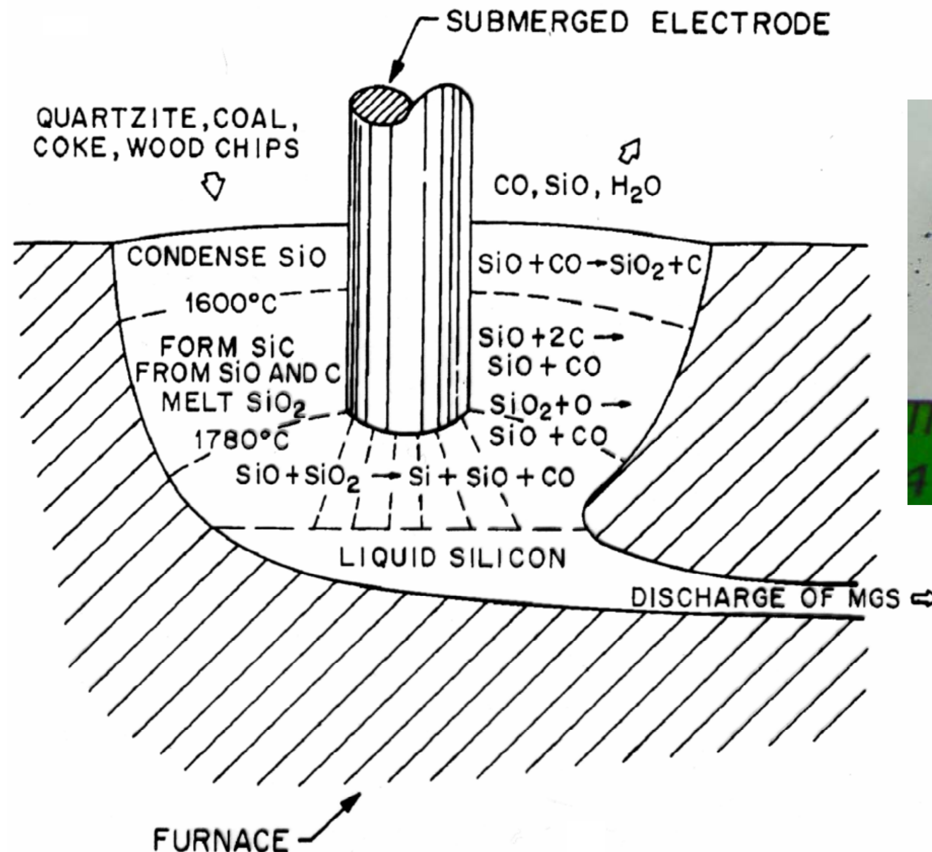
- diameter: 100 mm (4 inch) – 300 mm (12 inch)
- wafer thickness : 0.4 – 1 mm
- doping elements: B, Al, In, Ga: p-type doping (holes as majority)
  P, As, Sb: n-type doping (electrons as majority)

Physical parameter for Si:

- mobility: electrons: ca. 1250 cm^2/Vs
  holes: ca. 490 cm^2/Vs
- density: 2.33 g/cm^3
- melting point: 1423°C
- dielectric constant ε_{Si}: 11.8



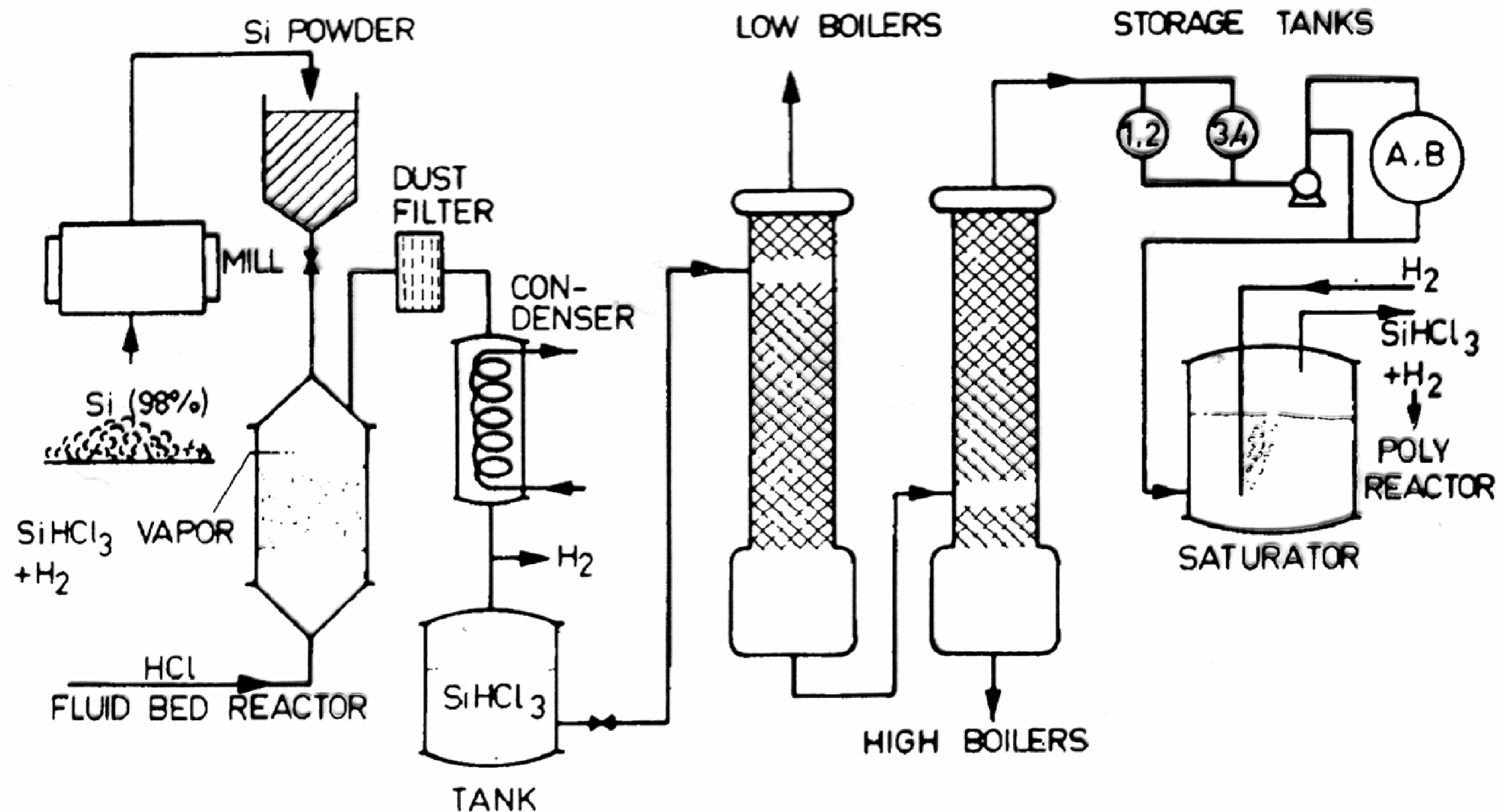
From Quarzite (sand) to pure Silicon



Reaction at 1500°C:

SiO_2 or SiOH + 2 C → Si + 2 CO (+H_2) results in liquid silicon and in „metallurgical grade silicon" (MGS), 98% Si

Purification of the MGS



Purification of Metallurgical Grade Silicon (MSG) with $SiHCl_3$

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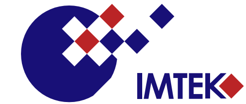
Fractional distillation



(1) vaporization (separation in the ´Low Boiler´, T = 31°C): Separation of liquid components by vaporization of $SiHCl_3$ (Trichlorsilan processing)

boiling point: BCl_3 (12°C), SiH_2Cl_2 (8°C)

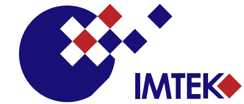
(2) step-down distillation (´High Boiler´, T = 33°C): Condensation of $SiHCl_3$

boiling point:

$FeCl_2$, $NiCl_2$	metallic, solid		
WCl_6	347°C	$TiCl_4$	136°C
$InCl_3$	300°C	$AsCl_3$	132°C
$SbCl_3$	283°C	$GeCl_4$	83°C
$GaCl_3$	203°C	PCl_3	76°C
$AlCl_3$	188°C	CCl_4	76°C
$SiHCl_3$	**32°C**		

➔ only $SiHCl_3$ evaporates, all others condensate

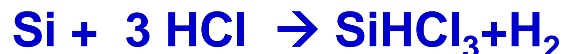
Summary: Si purification



(1) Reaction at 1500°C:

Sand or quarzite → liquid silicon

(2) Reaction at 300°C:

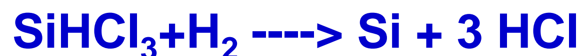


gaseous, boiling point 31.8°C

high purity $SiHCl_3$ is delivered by distillation

contamination < 10^{-9}

(3) Reverse Trichlorsilan Processing at 1000°C:

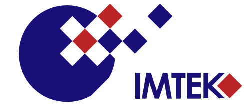


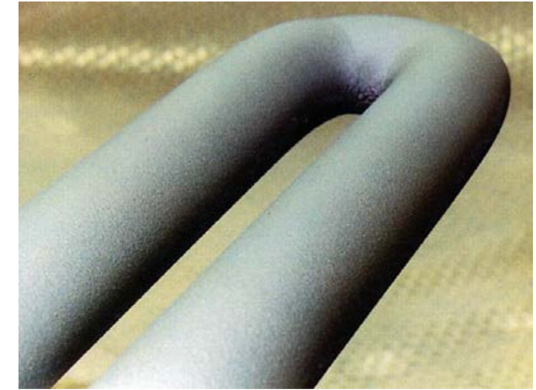
extraction of poly crystalline silicon rods (undoped)

Reduction of gaseous $SiHCl_3$ to solid silicon and gaseous HCl

→ undoped, high purity polycrystalline silicon

Reverse Trichlorsilan Processing



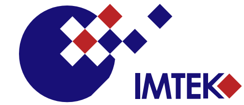


Poly silicon Rod

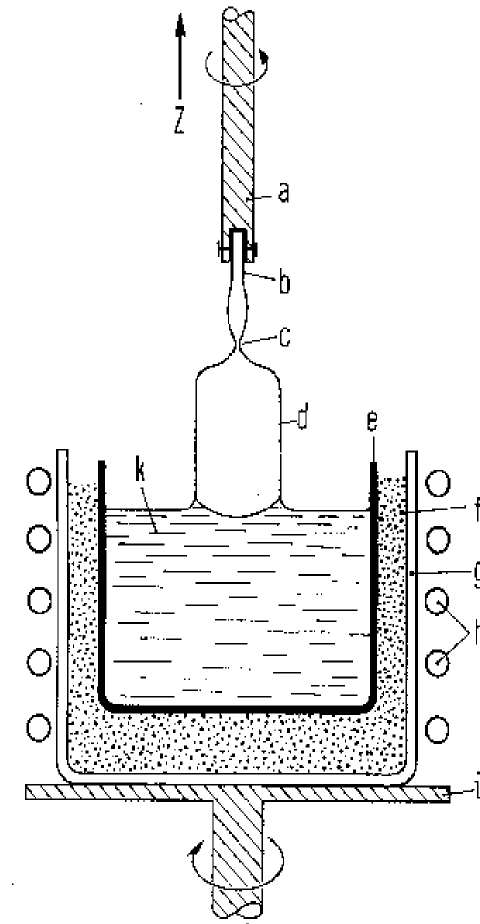
Reduction of gaseous $SiHCl_3$ to solid silicon and gaseous HCl at 1000°C

Poly silicon rods

Czochralski Growth of Silicon



Czochralski fab

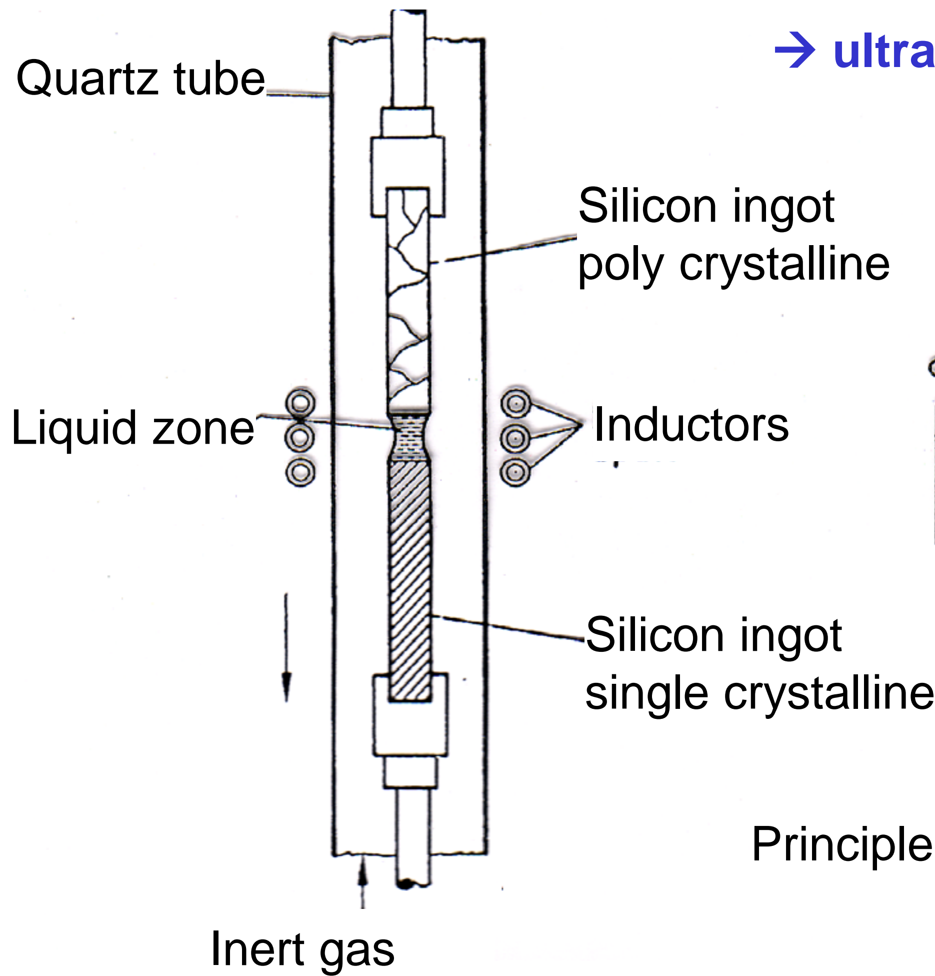


- melt & seed before crystallization
- beginning of the crystallization (increasingly diameter)
- growth with constant diameter

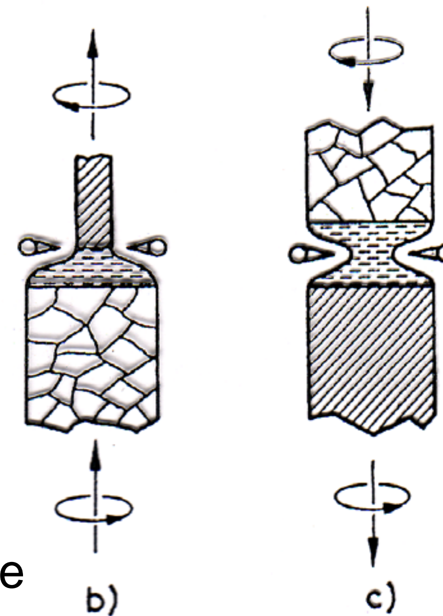
→oxygen rich silicon

Standard process for Si wafer production, “cheap” and reliable

Float zone Silicon

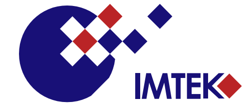


→ **ultra pure silicon**

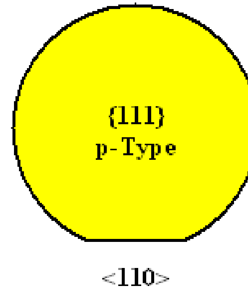


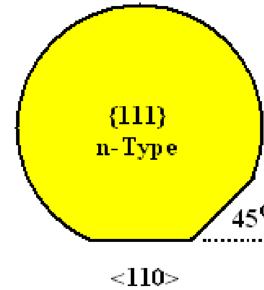
Principle of the floating-zone melting
a) general view (schematic)
b) „platform – process“
c) „bottle-neck – process“

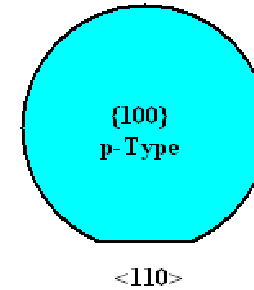
Processing the ingots

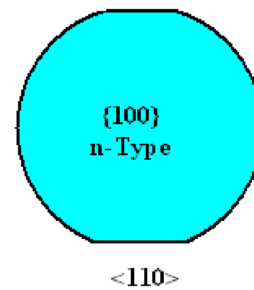


- **before cutting:** identification Of the ingots by 1 or 2 flats: primary and secondary flat

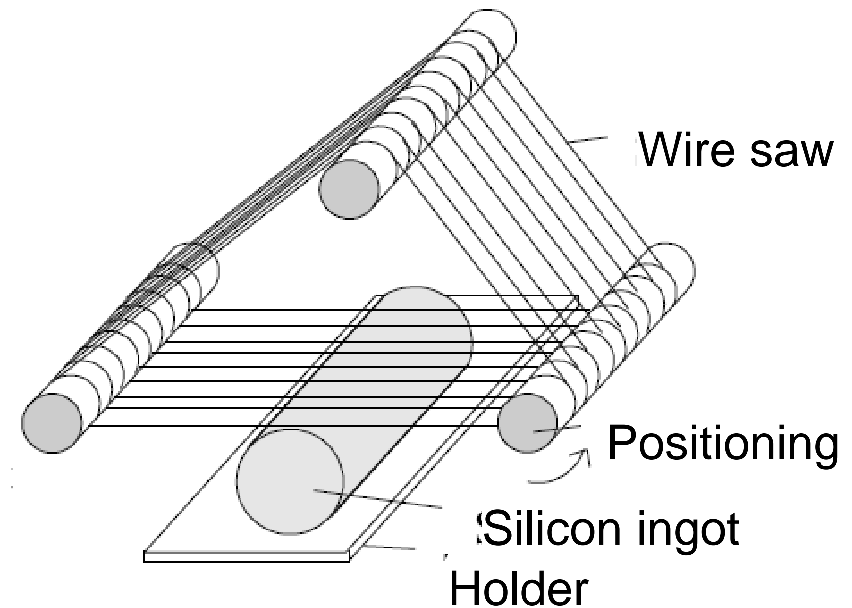


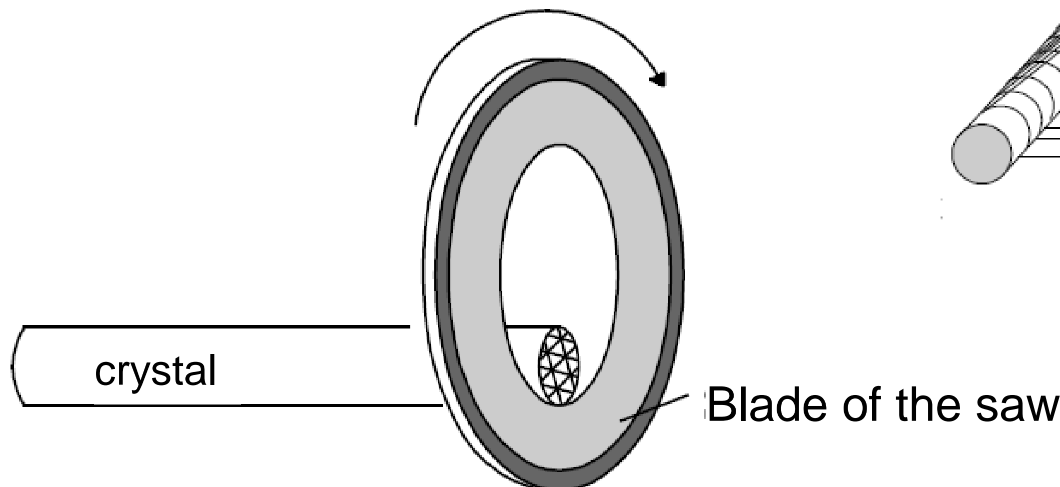






- **Cutting**: Blade with diamond powder, wire saw or center cutting blade saw Material loss about 300 µm/cut





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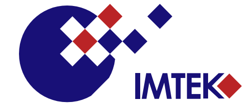
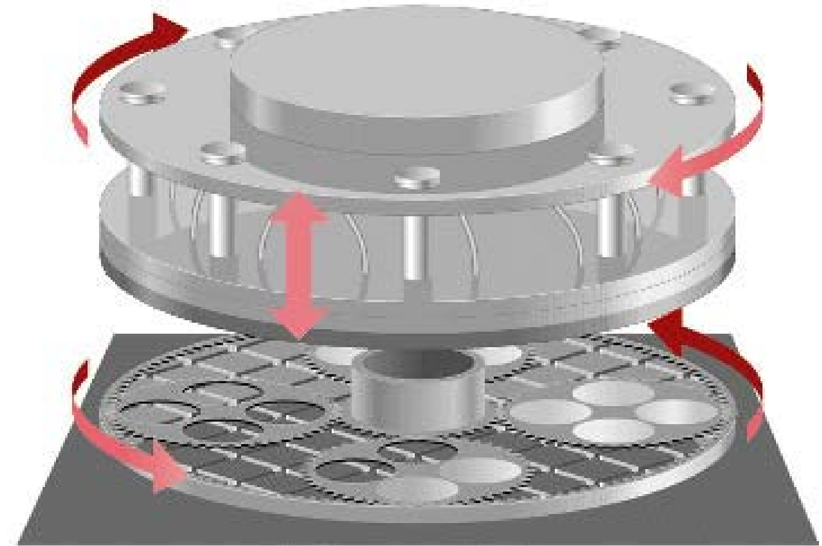
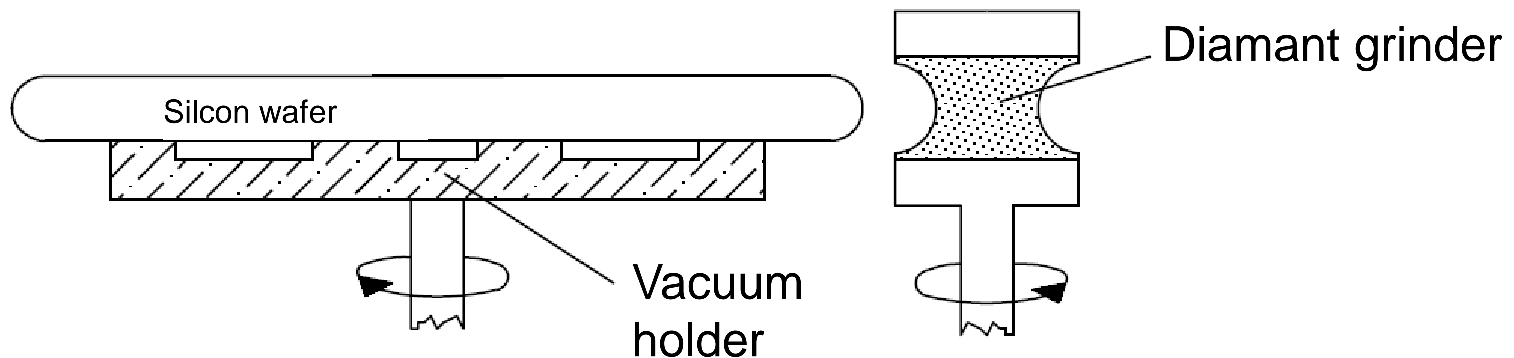
Processing the ingots



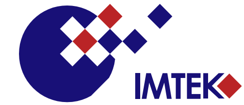
- **Wafer grinding (lapping)**:
  Aluminum oxide + Glycerin,
  reduction of 20-50 µm of
  the wafer
  surface flatness +/- 2 µm



- **Wafer edge rounding**:
  better handling,
  hinders a splitting of future films



Etching, polishing



- **Etching the wafer surface:**

  Etching of 20 µm Silicon in a solution of nitric acid ((HNO_3)), hydrofluoric acid (HF) and acetic acid (CH_3COOH)

  → To take away lattice damage and saw marks

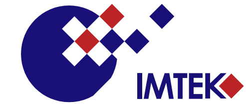
- **Polishing of the wafer surface:**

  $NaOH + H_2O + SiO_2$- Polish (10nm)
  (use of silicic acids)

  CMP: Chemical-Mechanical Polish done repeatedly with intermediate cleaning/rinsing with DI water

  → Takes away about 5 µm

Cleaning, rinsing, drying

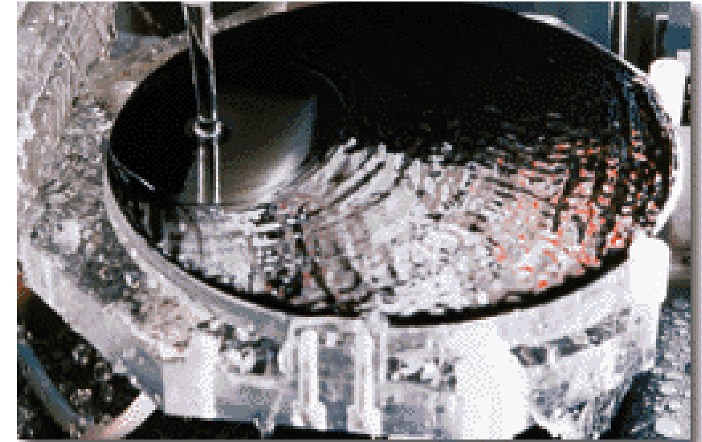


- **Cleaning:** 3 steps

(1) SC1 solution: ammonia (NH_3), hydrogen peroxide (H_2O_2) & ultra pure water (DI)
- removes all organics from surface

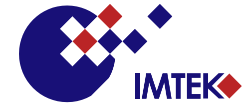
(2) HF dip: removes oxides and metal contaminations

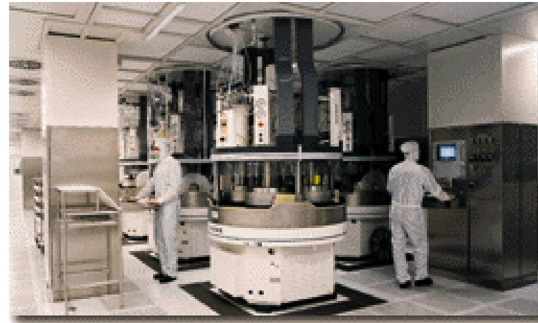
(3) SC2 solution: hydrochloric acid (HCl) and hydrogen peroxide (H_2O_2) grows a very pure oxide layer on top of the Si wafer



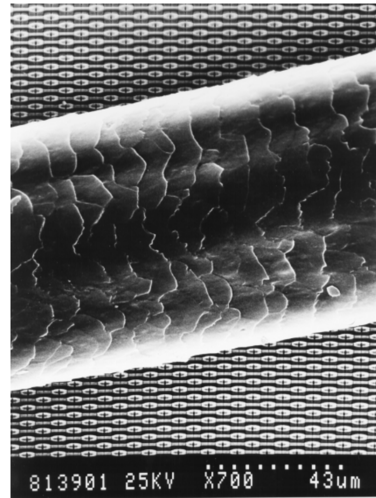
- **Rinse, drying:** Wet stations which allow the typical process like coating, etching, developing, cleaning, temperature controlled developing/rinsing/drying

Clean room processes



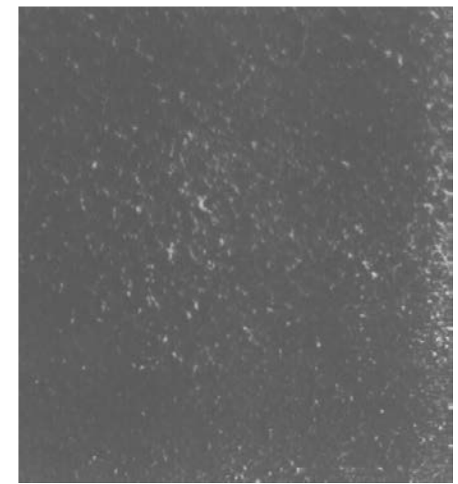


Dirt on a neck chain after one day of use



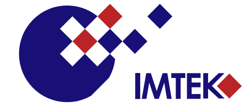
Hair compared to structures on chip

Xerox paper



Clean room paper

Clean room classification
(US Federal Standard 209d)



Particle number/ ft^3

10^6
10^5
10^4
10^3
10^2
10^1
10^0

class 100.000
class 10.000
class 1.000
class 100
class 10
class 1
Out door air

0.01 0.05 0.1 0.5 1.0 5 10 100

Particle size / µm