Cadence® Rapid Adoption Kits

Cadence Rapid Adoption Kits demonstrate how users can use their tools in their flows to improve productivity and to maximize the benefits of their tools. These packages can contain workshop databases or demo designs, instructional documents, overview presentations, deeper dive Application Notes and videos.

How to access the Rapid Adoption Kits?

To get started with the Rapid Adoption Kits, use the following link:

http://support.cadence.com/wps/myportal/cos/COSHome/resources/RapidAdoptionKits/
*Please note that a **support.cadence.com** account is required to access this content.*

There you will find all the related material, including documentation, videos and project files. The Rapid Adoption Kits are split into three sections:

Virtuoso® Custom IC and Sign-off Flow

These Rapid Adoption Kits are related to the **Virtuoso Custom IC and Sign-off Flow** using Virtuoso Schematic Editor (VSE), Multi-Mode Simulation (MMSIM), Virtuoso Layout Suite (VLS), Physical Verification System (PVS) and other Virtuoso products.

Encounter® Digital Implementation (EDI) System and Sign-off Flow

These Rapid Adoption Kits are related to the **Encounter Digital Implementation (EDI) System and Sign-off Flow** using Encounter Digital Implementation (EDI) System, Encounter Timing System (ETS) and Encounter Power System (EPS).

Synthesis, Test and Verification flow

These Rapid Adoption Kits are related to the **Synthesis, Test and Verification flow** using RTL Compiler, Encounter Test, Conformal, and Incisive products.

You can find more information about the available Rapid Adoption Kits below on this document, or on the landing page.

Virtuoso® Custom IC and Sign-off Flow

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Layout Design in IC 6.1.5

Faster, more accurate physical design using Virtuoso Schematic Editor and Virtuoso Layout Suite

This material highlights new features and explores some basic functionality with Virtuoso Schematic Editor L/XL and Virtuoso Layout Suite L/XL in the 6.1.5 release. You will take a design from concept through implementation and learn how Virtuoso 6.1.5 capabilities can help you generate designs more efficiently.

What you will learn:

- Increase designer productivity by leveraging connectivity throughout the design process
- Use ties between schematic capture and layout, commonly referred to as connectivity, to generate designs rapidly without sacrificing quality or performance

IC 6.1.5 Constraint Driven Custom Design

Optimized exchange between front-end and back-end designers for better layout productivity

The constraint-driven flow enables you to capture and transfer design requirements formally through the Constraint Management System, and then use automatic and interactive tools to enforce the requirements in the layout to ensure convergence on design goals. Constraints can be verified between front and back to ensure that the layout is using them as intended and that they have been implemented correctly. Finally, the system also enables storing and reusing of constraints across designs or projects.

What you will learn:

- Use the Constraint Management System
- Use the Circuit Prospector for assisted constraint capture
- Verify constraints to ensure that design intent is met in layout
- Use the module generation (MODGEN) capability for precision Pcell-based array generation
- Perform constraint-driven wire editing
- Perform constraint-aware editing
- Perform special net automated routing (differential pair, shielding, etc.)
- Perform full custom/analog placement

Virtuoso Visualization & Analysis (ViVA)

Analog/mixed-signal waveform viewing and analysis

The Virtuoso Visualization and Analysis tool is an analog/mixed-signal waveform viewer providing the means to thoroughly analyze the data generated by circuit simulation. Learn how to use it either as a standalone tool or as an integrated part of the Virtuoso Analog Design Environment (L and XL).

What you will learn:

- View, configure, and export design data in a variety of formats quickly and easily
- Interactively analyze and annotate waveform data for design documentation
- Create and evaluate complex mathematical expressions, and save them for later reuse
- How to efficiently handle gigabyte transient data files

IC6.1 Front to Back Overview

Complete front to back design flow in IC615

This material highlights the complete front to back design flow available in the IC615 release framing these capabilities in terms of designer productivity and results from the Metrics-driven Productivity Initiative (MPI).

What you will learn:

- Design creation and constraint capture in the Virtuoso Schematic Editor
- Design analysis and verification with the Analog Design Environment
- Constraints
- Virtuoso environment
- Buses
- Constraint aware editing
- Fluid guardring
- Virtuoso Spaced-based Router & interactive routing.

Guidelines on modeling analog circuits with WREAL

Modeling analog circuits with WREAL

This material illustrates wreal modeling concepts by migrating a Verilog-A based model of an AM modulation-demodulation system to a wreal model with Verilog-AMS. The wreal equivalent of each block will be created to build up an all digital simulation for system.

What you will learn:

- During the course of the example, guideline steps for creating wreal Verilog-AMS models will be developed and used for developing the wreal models
- The role of connect modules in a mixed-signal wreal simulation will be investigated
- The effects of sampling frequency will also be discussed, and the bilinear transform will be used to create a discrete time low pass filter

Introduction to AMS Designer Simulation

Introduction to AMS Designer Simulation

This material uses a simple database consisting of an inverter chain to show the setup and use of AMS Designer.

What you will learn:

- Both the GUI driven flow with ADE L and the text based command line flow are shown
- The steps to setup an AMS simulation in ADE L are discussed
- The ADE AMS Error Explanation tool will be used to show how to resolve simulation setup errors
- The steps needed to build the config view used in AMS simulation are illustrated
- The schematic based test case will be migrated to command line simulation to give an overview of both the runams and irun AMS command line based simulation flows

IC 6.1.5 Rapid Analog Prototyping (RAP) Workshop

IC 6.1.5 Rapid Analog Prototyping (RAP) Workshop

This material steps through a Rapid Analog Prototyping Flow in Virtuoso in IC 6.1.5. The objective of this flow is to generate the layout of an analog circuit in an automated manner, in order to obtain early feedback on parasitics and device effects on circuit simulation.

What you will learn:

- As a circuit designer you can thus identify issues early on and make necessary changes to quickly iterate through the flow which helps avoid costly changes late in the cycle and enables faster design convergence
- We demonstrate this flow using a sample and hold circuit based on a generic 45nm PDK

Parasitic Aware Design Workshop

Parasitic Aware Design (PAD) Workshop

ADE GXL's Parasitic Aware Design (PAD) features are used to investigate the effect of parasitic devices on a circuit. This material has been designed to highlight the features and functionality of the PAD flow in IC 6.1.5.

What you will learn:

- PAD Flow Overview
- Estimated Parasitic Flow
- Extracted Parasitic Flow
- Parasitic Reporting Flow
- Estimated PAD Flow using Custom Parasitic Cells

Analog Design Environment XL (ADE XL) Workshop

Analog Design Environment XL (ADE XL) Workshop

Virtuoso Analog Design Environment XL provides a multi-test simulation environment for thorough design validation, extensive design exploration, IP reuse, and early insight into manufacturing variability. This material has been designed to highlight many of the features and functionality of ADE XL.

What you will learn:

- Use Analog Design Environment XL to efficiently manage all your simulations and to easily access all results
- Validate designs thoroughly over all required corners
- Automatically create design documentation based on results
- Use Analog Design Environment XL for improved verification coverage and statistical analysis

Encounter® Digital Implementation (EDI) System and Sign-off Flow

*These Rapid Adoption Kits are related to the **Encounter Digital Implementation (EDI) System and Sign-off Flow** using Encounter Digital Implementation (EDI) System, Encounter Timing System (ETS) and Encounter Power System (EPS).*

Clock Concurrent Optimization (CCOpt)

What you will learn:

- Basics of running clock concurrent optimization (CCOpt) on a design in Encounter Digital Implementation (EDI) system
- How to configure number of settings that control, how CCOpt will optimize the design
- How to run standalone CCOpt and use its analysis tools to investigate the design
- Advanced design debug techniques with CCOpt
- How to generate RC multipliers by correlating SPEF values with estimates for existing nets

Database Access with DBTCL

What you will learn:

- dbGet basics: interactive queries and introduction to database traversal in Encounter Digital Implementation (EDI) system
- Advanced dbGet techniques for programming using pattern matching to filter lists of pointers
- Using dbGet .?h and dbSchema to learn more about the database objects and their attributes
- Modifying object attributes using dbSet

Post Assembly Closure (PAC) Flow

What you will learn:

- Basics of running Post Assembly Closure (PAC) flow on a design in Encounter Digital Implementation (EDI) system
- To assemble the design and libraries into the Encounter Digital Implementation system and create a floorplan
- To enable the PAC mode
- Verify the correctness of the data

Prototyping Foundation Flat Flow

What you will learn:

- Gigascale Prototyping with FlexModels
- Prototyping Usage Model.
- FlexModels enable GigaScale Design Exploration using EDI System

Prototyping Foundation Top to Bottom Flow

What you will learn:

- Gigascale Prototyping with FlexModels
- Prototyping Usage Model
- FlexModels enable GigaScale Design Exploration using EDI System

Encounter Low-Power Design Flow: CPF Implementation

What you will learn:

- How LP Foundation Flow works
- The advantage of CPF to implement designs with multiple supply voltage (MSV) and power shut-off (PSO) architecture
- Setting up MMMC in Low Power Flow

MMMC SignOff ECO using EDI System and ETS

What you will learn:

- Overview and context
- What is the MMMC SignOff ECO solution
- Use model
- Results on several customer designs

Global Timing Debug using EDI System or ETS

What you will learn:

- Use Model
- How to use global timing debug utility to do timing analysis
- How to create different categories for timing analysis
- How to perform bottleneck analysis

Synthesis, Test and Verification flow

*These Rapid Adoption Kits are related to the **Synthesis, Test and Verification flow** using RTL Compiler, Encounter Test, Conformal, and Incisive products.*

RTL Compiler: 11.1 Adoption Kit

Includes RTL Compiler (RC) Rapid Adoption Kit with demo design. Provides detailed RC overview, how to get started and create a simple script quickly, insights into smart debugging, and general understanding of RC's flexible TCL infrastructure for increased productivity.

Skill Level : Beginner

RTL Compiler and Conformal LEC: Getting the Best out of RC and LEC

Includes RTL Compiler(RC) and Conformal LEC(LEC) and Rapid Adoption Kit with demo design (design embedded within tool release, instructions are provided on how to setup user environment). Introduces new framework to help RC/LEC verification.

Skill Level : Beginner

RTL Compiler(RC) and Incisive: RTL Power Profiling

Includes RTL Compiler (RC) and Incisive (IES) Rapid Adoption Kit with demo design. Demonstrates how users can leverage both synthesis and verification technologies to perform early accurate power analysis.

Skill Level : Intermediate

RTL Compiler Physical: Physically-aware Timing Closure and Congestion Analysis

Includes RC Physical (RCP) Rapid Adoption Kit with demo design. Demonstrates physically-aware timing closure and congestion analysis. Hand off fully-placed and legalized seed placement to physical design.

Skill Level : Intermediate

RTL Compiler Physical and Encounter Test: Physically-aware DFT

Includes RTL Compiler Physical (RCP) and Encounter Test (ET) Rapid Adoption Kit with demo design. Introduces benefits of physically-aware test synthesis driving predictability.

Skill Level : Intermediate

Conformal Low Power, RTL Compiler and Incisive: Low Power Verification for Beginners

Includes Rapid Adoption Kit with demo design (instructions are provided on how to setup user environment). Introduces closed loop verification methodology using Conformal Low Power.

Skill Level : Beginner

Conformal Low Power and RTL Compiler: Low Power Verification for Advanced Users

Includes Rapid Adoption Kit with demo design (instructions are provided on how to setup user environment). Introduces advanced features of Conformal Low Power – Power Intent Comparison, Hierarchical Integration and CPF Macro Modeling.

Skill Level : Intermediate

Conformal Constraint Designer: SDC Constraint and CDC Verification Methodologies

Includes Conformal Constraint Designer (CCD) Rapid Adoption Kit with demo design. Demonstrates how users can perform SDC constraint checks and Clock Domain Crossing (CDC) checks application for both IP and chip-level requirements.

Skill Level : Beginner

Conformal ECO Designer and EDI System: Enabling RTL-to-GDSII ECO Flows

Includes Conformal ECO Designer(ECO) and EDI Rapid Adoption Kit with demo design. Steps through RTL-to-GDSII ECO flows users can leverage for their own design environment. Demonstrates benefits of leveraging RTL Compiler under-the-hood for auto delta logic synthesis - transparent to user.

Skill Level : Beginner

Conformal Low Power: CPF Macro Models

Includes Conformal Low Power (CLP) Rapid Adoption Kit with demo design. Demonstrates benefits of CPF macro modeling that can be leveraged throughout the Cadence low power design flow for increased productivity.

Skill Level : Intermediate

Conformal Low Power: UPF-to-CPF Translation and Low Power Verification

Includes Conformal Low Power (CLP) Rapid Adoption Kit with demo design. Introduces the low power interoperability flow using CLP and how to convert UPF to CPF. Included are guidance and recommendations to navigate around some of the pitfalls of mixed-format flow.

Skill Level : Intermediate

RTL Compiler and Conformal Low Power: Advanced Low Power Synthesis Validation

Includes RTL Compiler (RC) and Conformal Low power (CLP) Rapid Adoption Kit with demo low power design and labs. Demonstrates how users can leverage RTL compiler to perform multi-supply voltage (MSV) synthesis and low power cell insertion for power shutoff (PSO) and MSV. The RAK also demonstrates the use of Conformal low power to validate power intent (CPF) quality and the synthesized design netlist for equivalence and electrical integrity.

Skill Level : Intermediate

Conformal LEC: LEC Jumpstart Kit

Includes LEC Jumpstart Kit with demo design and lab instructions. Provides detailed LEC technical step-by-step guide, how to get started and create a simple script quickly, insights into smart debugging, and general understanding of LEC's terminology and best practices for increased productivity.

Skill Level : Beginner

Encounter Test and RTL Compiler: Integrating DFT during Synthesis

Includes RTL Compiler (RC) and Encounter Test (ET) Rapid Adoption Kit with demo design. Helps user walk through several of the DFT capabilities available for insertion via RC, including testability analysis, compression analysis and insertion, and MBIST insertion. Shows the link to ET and how that flow is run.

Skill Level : Beginner

Encounter Test: Low Power ATPG

Includes Encounter Test (ET) Rapid Adoption Kit with demo design. Demonstrates the Low Power ATPG flow in Encounter Test. Describes how the flow is used to analyze the toggle activity and set the proper options to generate ATPG patterns that will not only lower the toggle activity, but also stress the chip properly for manufacturing test.

Skill Level : Intermediate

Encounter Test: Precision Diagnostics

Includes Encounter Test (ET) Rapid Adoption Kit with demo design. Demonstrates how ET ATPG customers can step through the precision diagnostics flow using Encounter Diagnostics.

Skill Level : Advanced

Encounter Test and RTL Compiler: Adding Structured Test and ATPG in the VDI Environment

Includes Encounter Test (ET) and Virtuoso Digital Implementation (VDI) system Rapid Adoption Kit with demo design. Demonstrates how VDI customers can use RTL Compiler (RC) to create designs ready for structured test so mixed-signal designers can get familiar with the flow of using RC to insert scan and test points and then run ATPG using ET.

Skill Level : Intermediate